When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog output is the current i_O. V_{ref} is a constant reference voltage.

(a) Show that

$$i_O = \frac{V_{ref}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

(b) Which bit is the LSB? Which is the MSB?

(c) For $V_{ref} = 10$ V, $R = 10$ kΩ, and $N = 8$, find the maximum value of i_O obtained. What is the change in i_O resulting from the LSB changing from 0 to 1?

1.38 In compact-disc (CD) audio technology, the audio signal is sampled at 44.1 kHz. Each sample is represented by 16 bits. What is the speed of this system in bits per second?

Section 1.4: Amplifiers

1.39 Various amplifier and load combinations are measured as listed below using rms values. For each, find the voltage, current, and power gains (A_v, A_i, and A_p, respectively) both as ratios and in dB:

(a) $v_I = 100$ mV, $i_I = 100$ μA, $v_O = 10$ V, $R_L = 100$ Ω
(b) $v_I = 10$ μV, $i_I = 100$ nA, $v_O = 1$ V, $R_L = 10$ kΩ
(c) $v_I = 1$ V, $i_I = 1$ mA, $v_O = 5$ V, $R_L = 10$ Ω

1.40 An amplifier operating from ±3-V supplies provides a 2.2-V peak sine wave across a 100-Ω load when provided with a 0.2-V peak input from which 1.0 mA peak is drawn. The average current in each supply is measured to be 20 mA. Find the voltage gain, current gain, and power gain expressed as ratios and in decibels as well as the supply power, amplifier dissipation, and amplifier efficiency.

1.41 An amplifier using balanced power supplies is known to saturate for signals extending within 1.0 V of either supply. For linear operation, its gain is 200 V/V. What is the rms value of the largest undistorted sine-wave output available, and input needed, with ±5-V supplies? With ±10-V supplies? With ±15-V supplies?

1.42 Symmetrically saturating amplifiers, operating in the so-called clipping mode, can be used to convert sine waves to pseudo-square waves. For an amplifier with a small-signal gain of 1000 and clipping levels of ±10 V, what peak value of input sinusoid is needed to produce an output whose extremes are just at the edge of clipping? Clipped 90% of the time? Clipped 99% of the time?

Section 1.5: Circuit Models for Amplifiers

1.43 Consider the voltage-amplifier circuit model shown in Fig. 1.16(b), in which $A_{vo} = 100$ V/V under the following conditions:

(a) $R_i = 10R_s$, $R_L = 10R_o$
(b) $R_i = R_s$, $R_L = R_o$
(c) $R_i = R_s/10$, $R_L = R_o/10$

Calculate the overall voltage gain v_o/v_s in each case, expressed both directly and in decibels.

1.44 An amplifier with 40 dB of small-signal, open-circuit voltage gain, an input resistance of 1 MΩ, and an output resistance of 100 Ω, drives a load of 500 Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of 20 mA, what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

1.45 A 10-mV signal source having an internal resistance of 100 kΩ is connected to an amplifier for which the input resistance is 10 kΩ, the open-circuit voltage gain is 1000 V/V, and the output resistance is 1 kΩ. The amplifier is connected in turn to a 100-Ω load. What overall voltage gain results as measured from the source internal voltage to the load? Where did all the gain go? What would the gain be if the source was connected directly to the load? What is the ratio of these two gains? This ratio is a useful measure of the benefit the amplifier brings.

1.46 A buffer amplifier with a gain of 1 V/V has an input resistance of 1 MΩ and an output resistance of 20 Ω. It is connected between a 1-V, 200-kΩ source and a 100-Ω

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

load. What load voltage results? What are the corresponding voltage, current, and power gains (in dB)?

1.47 Consider the cascade amplifier of Example 1.3. Find the overall voltage gain v_o/v_s obtained when the first and second stages are interchanged. Compare this value with the result in Example 1.3, and comment.

1.48 You are given two amplifiers, A and B, to connect in cascade between a 10-mV, 100-kΩ source and a 100-Ω load. The amplifiers have voltage gain, input resistance, and output resistance as follows: for A, 100 V/V, 100 kΩ, 10 kΩ, respectively; for B, 10 V/V, 10 kΩ, 1 kΩ, respectively. Your problem is to decide how the amplifiers should be connected. To proceed, evaluate the two possible connections between source S and load L, namely, SABL and SBAL. Find the voltage gain for each both as a ratio and in decibels. Which amplifier arrangement is best?

D *1.49 A designer has available voltage amplifiers with an input resistance of 10 kΩ, an output resistance of 1 kΩ, and an open-circuit voltage gain of 10. The signal source has a 10-kΩ resistance and provides a 5-mV rms signal, and it is required to provide a signal of at least 3 V rms to a 200-Ω load. How many amplifier stages are required? What is the output voltage actually obtained?

D *1.50 Design an amplifier that provides 0.5 W of signal power to a 100-Ω load resistance. The signal source provides a 30-mV rms signal and has a resistance of 0.5 MΩ. Three types of voltage-amplifier stages are available:

(a) A high-input-resistance type with $R_i = 1$ MΩ, $A_{vo} = 10$, and $R_o = 10$ kΩ
(b) A high-gain type with $R_i = 10$ kΩ, $A_{vo} = 100$, and $R_o = 1$ kΩ
(c) A low-output-resistance type with $R_i = 10$ kΩ, $A_{vo} = 1$, and $R_o = 20$ Ω

Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of stages and should ensure that the signal level is not reduced below 10 mV at any point in the amplifier chain. Find the load voltage and power output realized.

D *1.51 It is required to design a voltage amplifier to be driven from a signal source having a 5-mV peak amplitude and a source resistance of 10 kΩ to supply a peak output of 2 V across a 1-kΩ load.

(a) What is the required voltage gain from the source to the load?
(b) If the peak current available from the source is 0.1 μA, what is the smallest input resistance allowed? For the design with this value of R_i, find the overall current gain and power gain.
(c) If the amplifier power supply limits the peak value of the output open-circuit voltage to 3 V, what is the largest output resistance allowed?
(d) For the design with R_i as in (b) and R_o as in (c), what is the required value of open-circuit voltage gain, i.e., $\left.\frac{v_o}{v_i}\right|_{R_{L=\infty}}$, of the amplifier?
(e) If, as a possible design option, you are able to increase R_i to the nearest value of the form 1×10^n Ω and to decrease R_o to the nearest value of the form 1×10^m Ω, find (i) the input resistance achievable; (ii) the output resistance achievable; and (iii) the open-circuit voltage gain now required to meet the specifications.

D 1.52 A voltage amplifier with an input resistance of 20 kΩ, an output resistance of 100 Ω, and a gain of 1000 V/V is connected between a 100-kΩ source with an open-circuit voltage of 10 mV and a 100-Ω load. For this situation:

(a) What output voltage results?
(b) What is the voltage gain from source to load?
(c) What is the voltage gain from the amplifier input to the load?
(d) If the output voltage across the load is twice that needed and there are signs of internal amplifier overload, suggest the location and value of a single resistor that would produce the desired output. Choose an arrangement that would cause minimum disruption to an operating circuit. (*Hint:* Use parallel rather than series connections.)

1.53 A voltage amplifier delivers 200 mV across a load resistance of 1 kΩ. It was found that the output voltage decreases by 5 mV when R_L is decreased to 780 Ω. What are the values of the open-circuit output voltage and the output resistance of the amplifier?

1.54 A current amplifier supplies 1 mA to a load resistance of 1 kΩ. When the load resistance is increased to 12 kΩ, the output current decreases to 0.5 mA. What are the values of the short-circuit output current and the output resistance of the amplifier?

1.55 A current amplifier for which $R_i = 100\ \Omega$, $R_o = 10\ \text{k}\Omega$, and $A_{is} = 100$ A/A is to be connected between a 100-mV source with a resistance of 10 kΩ and a load of 1 kΩ. What are the values of current gain i_o/i_i, of voltage gain v_o/v_s, and of power gain expressed directly and in decibels?

1.56 A transconductance amplifier with $R_i = 2\ \text{k}\Omega$, $G_m = 60$ mA/V, and $R_o = 20\ \text{k}\Omega$ is fed with a voltage source having a source resistance of 1 kΩ and is loaded with a 1-kΩ resistance. Find the voltage gain realized.

D **1.57** A designer is required to provide, across a 10-kΩ load, the weighted sum, $v_O = 10v_1 + 20v_2$, of input signals v_1 and v_2, each having a source resistance of 10 kΩ. She has a number of transconductance amplifiers for which the input and output resistances are both 10 kΩ and $G_m = 20$ mA/V, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. Your design should utilize the minimum number of amplifiers and resistors. (*Hint*: In your design, arrange to add currents.)

1.58 Figure P1.58 shows a transconductance amplifier whose output is *fed back* to its input. Find the input resistance R_{in} of the resulting one-port network. (*Hint*: Apply a test voltage v_x between the two input terminals, and find the current i_x drawn from the source. Then, $R_{\text{in}} \equiv v_x/i_x$.)

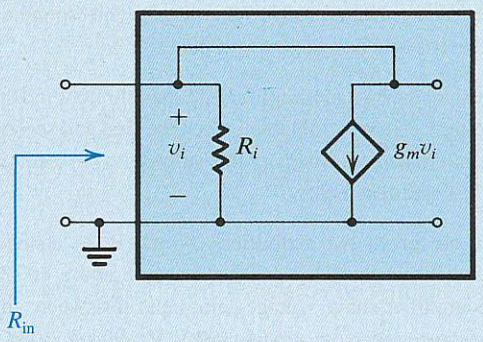

Figure P1.58

D **1.59** It is required to design an amplifier to sense the open-circuit output voltage of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Also, the load resistance varies in the range of 1 kΩ to 10 kΩ. The change in load voltage corresponding to the specified change in R_s should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in R_L should be limited to 10%. Also, corresponding to a 10-mV transducer open-circuit output voltage, the amplifier should provide a minimum of 1 V across the load. What type of amplifier is required? Sketch its circuit model, and specify the values of its parameters. Specify appropriate values for R_i and R_o of the form $1 \times 10^m\ \Omega$.

D **1.60** It is required to design an amplifier to sense the short-circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1 kΩ to 10 kΩ. Similarly, the load resistance is known to vary over the range of 1 kΩ to 10 kΩ. The change in load current corresponding to the specified change in R_s is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in R_L

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

2.2 The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain A. Measurements indicate $v_O = 4.0$ V when $v_I = 1.0$ V. What is the op-amp gain A?

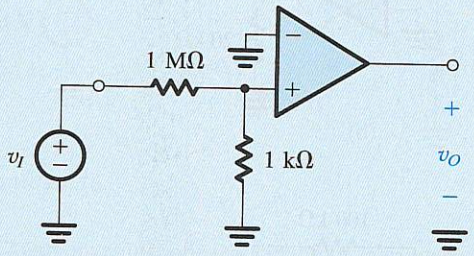

Figure P2.2

2.3 Measurement of a circuit incorporating what is thought to be an ideal op amp shows the voltage at the op-amp output to be −2.000 V and that at the negative input to be −1.000 V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is −1.005 V, what is likely to be the actual gain of the amplifier?

2.4 A set of experiments is run on an op amp that is ideal except for having a finite gain A. The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	v_1	v_2	v_O
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	−0.99
6	1.99	2.00	1.00
7	5.10		−5.10

2.5 Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances G_m and a transresistance R_m, find an expression for the open-loop gain A. For $G_m = 40$ mA/V and $R_m = 1 \times 10^6\ \Omega$, what value of A results?

2.6 The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 2-V sinusoid. The output signal of the transducer is sinusoidal of 5-mV amplitude and 1000-Hz frequency. Give expressions for v_{cm}, v_d, and the total signal between each wire and the system ground.

2.7 Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_O = A_d v_{Id} + A_{cm} v_{Icm}$$

where A_d is the differential gain (referred to simply as A in the text) and A_{cm} is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch ΔG_m between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \tfrac{1}{2}\Delta G_m$$

$$G_{m2} = G_m + \tfrac{1}{2}\Delta G_m$$

Find expressions for A_d, A_{cm}, and CMRR. What is the maximum permitted percentage mismatch between the two G_m values if a minimum CMRR of 60 dB is required?

Section 2.2: The Inverting Configuration

2.8 Assuming ideal op amps, find the voltage gain v_o/v_i and input resistance R_{in} of each of the circuits in Fig. P2.8.

2.9 A particular inverting circuit uses an ideal op amp and two 10-kΩ resistors. What closed-loop gain would you expect? If a dc voltage of +1.00 V is applied at the input, what outputs result? If the 10-kΩ resistors are said to be "1% resistors," having values somewhere in the range (1 ± 0.01) times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 1.00 V?

(b) Find the currents I_1, I_2, I_3, and I_4, in terms of the input current I.
(c) Find the voltages at nodes 1, 2, 3, and 4, that is, V_1, V_2, V_3, and V_4 in terms of (IR).

2.32 The circuit in Fig. P2.32 utilizes an ideal op amp.

(a) Find I_1, I_2, I_3, I_L, and V_x.
(b) If V_O is not to be lower than -13 V, find the maximum allowed value for R_L.
(c) If R_L is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in I_L and in V_O?

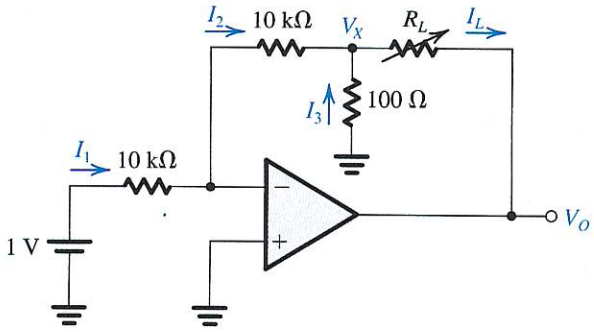

Figure P2.32

D 2.33 Use the circuit in Fig. P2.32 as an inspiration to design a circuit that supplies a constant current I_L of 3.1 mA to a variable resistance R_L. Assume the availability of a 1.5-V battery and design so that the current drawn from the battery is 0.1 mA. For the smallest resistance in the circuit, use 500 Ω. If the op amp saturates at ±10 V, what is the maximum value that R_L can have while the current source supplying it operates properly?

D 2.34 Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.34 to implement a current amplifier with gain $i_L/i_I = 11$ A/A.

(a) Find the required value for R.
(b) What are the input and the output resistance of this current amplifier?
(c) If $R_L = 1$ kΩ and the op amp operates in an ideal manner as long as v_O is in the range ±12 V, what range of i_I is possible?
(d) If the amplifier is fed with a current source having a current of 0.2 mA and a source resistance of 10 kΩ, find i_L.

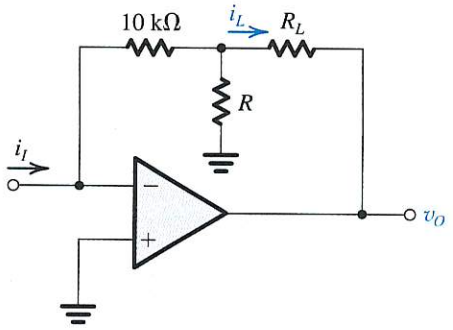

Figure P2.34

D 2.35 Design the circuit shown in Fig. P2.35 to have an input resistance of 100 kΩ and a gain that can be varied from -1 V/V to -100 V/V using the 100-kΩ potentiometer R_4. What voltage gain results when the potentiometer is set exactly at its middle value?

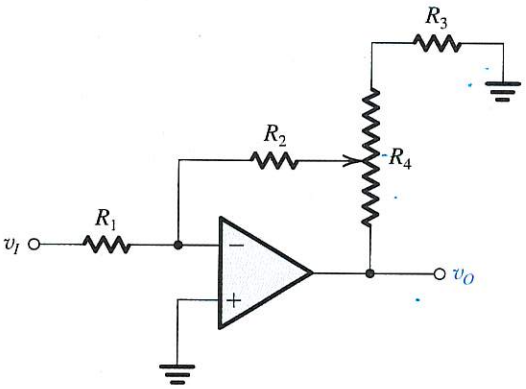

Figure P2.35

2.36 A weighted summer circuit using an ideal op amp has three inputs using 10-kΩ resistors and a feedback resistor of 50 kΩ. A signal v_1 is connected to two of the inputs while a signal v_2 is connected to the third. Express v_O in terms of v_1 and v_2. If $v_1 = 1$ V and $v_2 = -1$ V, what is v_O?

D 2.37 Design an op-amp circuit to provide an output $v_O = -[2v_1 + (v_2/2)]$. Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed 50 μA for 1-V input signals.

D 2.38 Use the scheme illustrated in Fig. 2.10 to design an op-amp circuit with inputs v_1, v_2, and v_3, whose output is

either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

D 2.46 Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage V applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100 μA, find the value of R such that a full-scale reading is obtained when V is +10 V. Does the meter resistance shown affect the voltmeter calibration?

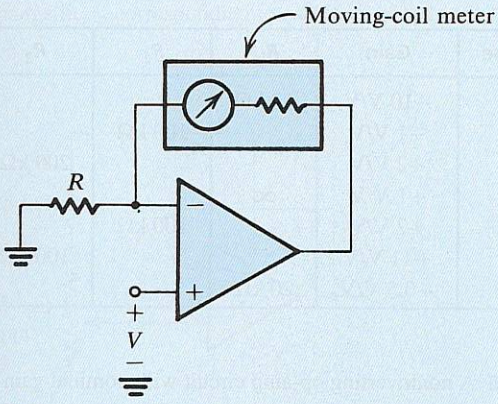

Figure P2.46

D *2.47 (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = \left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_P}{R_{P1}}v_{P1} + \frac{R_P}{R_{P2}}v_{P2} + \cdots + \frac{R_P}{R_{Pn}}v_{Pn}\right]$$

where $R_N = R_{N1} \| R_{N2} \| \cdots \| R_{Nn}$, and

$$R_P = R_{P1} \| R_{P2} \| \cdots \| R_{Pn} \| R_{P0}$$

(b) Design a circuit to obtain

$$v_O = -4v_{N1} + v_{P1} + 3v_{P2}$$

The smallest resistor used should be 10 kΩ.

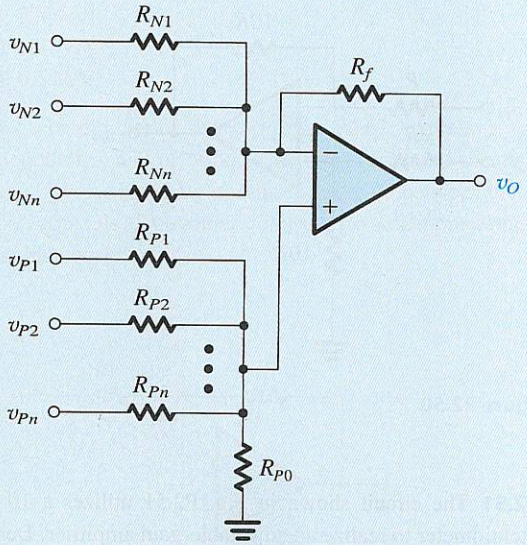

Figure P2.47

D *2.48 Design a circuit, using one ideal op amp, whose output is $v_O = v_{I1} + 2v_{I2} - 9v_{I3} + 4v_{I4}$. (*Hint:* Use a structure similar to that shown in general form in Fig. P2.47.)

2.49 Derive an expression for the voltage gain, v_O/v_I, of the circuit in Fig. P2.49.

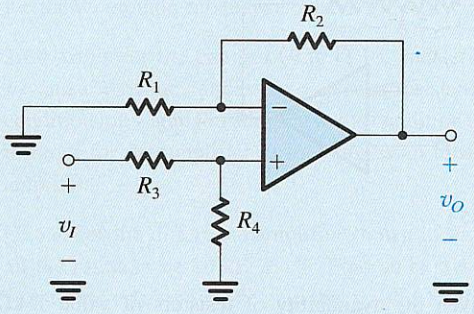

Figure P2.49

2.50 For the circuit in Fig. P2.50, use superposition to find v_O in terms of the input voltages v_1 and v_2. Assume an ideal op amp. For

$$v_1 = 10\sin(2\pi \times 60t) - 0.1\sin(2\pi \times 1000t), \text{ volts}$$
$$v_2 = 10\sin(2\pi \times 60t) + 0.1\sin(2\pi \times 1000t), \text{ volts}$$

find v_O.

where K is the nominal (ideal) value of the ratios (R_2/R_1) and (R_4/R_3). Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used. What resistor tolerance is needed if a CMRR of 80 dB is required?

D ***2.67** Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 1000, a differential input resistance of 2 kΩ, and a minimum CMRR of 88 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than x%).

***2.68** (a) Find A_d and A_{cm} for the difference amplifier circuit shown in Fig. P2.68.

(b) If the op amp is specified to operate properly as long as the common-mode voltage at its positive and negative inputs falls in the range ±2.5 V, what is the corresponding limitation on the range of the input common-mode signal v_{Icm}? (This is known as the **common-mode range** of the differential amplifier.)

(c) The circuit is modified by connecting a 10-kΩ resistor between node A and ground, and another 10-kΩ resistor between node B and ground. What will now be the values of A_d, A_{cm}, and the input common-mode range?

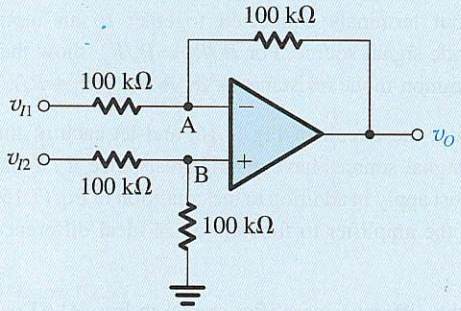

Figure P2.68

D ***2.69** To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor R connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5, R_6) connected across the output feeds a fraction β of the output, that is, a voltage βv_O, back to the positive-input terminal of the op amp through a resistor R. Assume that R_5 and R_6 are much smaller than R so that the current through R is much lower than the current in the voltage divider, with the result that $\beta \simeq R_6/(R_5 + R_6)$. Show that the differential gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{1}{1-\beta}$$

(*Hint:* Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of 2 MΩ. Select values for R, R_5, and R_6, such that $(R_5 + R_6) \leq R/100$.

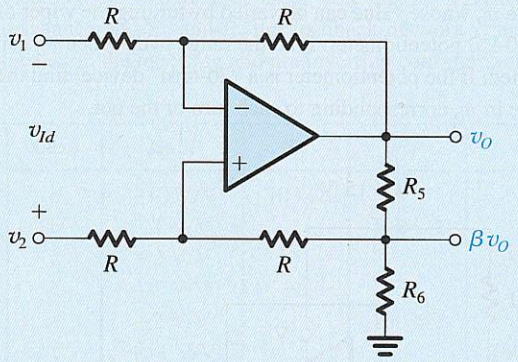

Figure P2.69

***2.70** Figure P2.70 shows a modified version of the difference amplifier. The modified circuit includes a resistor R_G, which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_O}{v_{Id}} = -2\frac{R_2}{R_1}\left[1 + \frac{R_2}{R_G}\right]$$

(*Hint:* The virtual short circuit at the op-amp input causes the current through the R_1 resistors to be $v_{Id}/2R_1$).

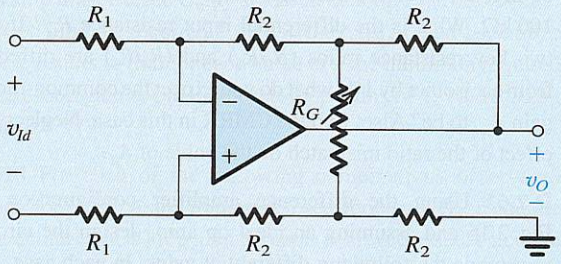

Figure P2.70

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem