2.2 The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain A. Measurements indicate $v_O = 4.0$ V when $v_I = 1.0$ V. What is the op-amp gain A?

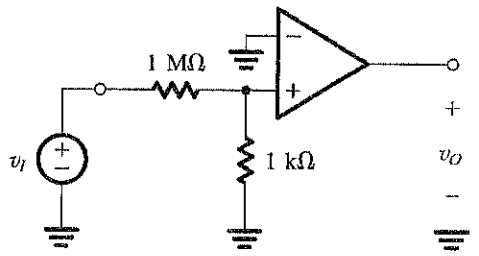

Figure P2.2

2.3 Measurement of a circuit incorporating what is thought to be an ideal op amp shows the voltage at the op-amp output to be −2.000 V and that at the negative input to be −1.000 V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is −1.005 V, what is likely to be the actual gain of the amplifier?

2.4 A set of experiments is run on an op amp that is ideal except for having a finite gain A. The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	v_1	v_2	v_O
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	−0.99
6	1.99	2.00	1.00
7	5.10		−5.10

2.5 Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances G_m and a transresistance R_m, find an expression for the open-loop gain A. For $G_m = 40$ mA/V and $R_m = 1 \times 10^6\ \Omega$, what value of A results?

2.6 The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 2-V sinusoid. The output signal of the transducer is sinusoidal of 5-mV amplitude and 1000-Hz frequency. Give expressions for v_{cm}, v_d, and the total signal between each wire and the system ground.

2.7 Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_O = A_d v_{id} + A_{cm} v_{icm}$$

where A_d is the differential gain (referred to simply as A in the text) and A_{cm} is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch ΔG_m between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \tfrac{1}{2}\Delta G_m$$

$$G_{m2} = G_m + \tfrac{1}{2}\Delta G_m$$

Find expressions for A_d, A_{cm}, and CMRR. What is the maximum permitted percentage mismatch between the two G_m values if a minimum CMRR of 60 dB is required?

Section 2.2: The Inverting Configuration

2.8 Assuming ideal op amps, find the voltage gain v_o/v_i and input resistance R_{in} of each of the circuits in Fig. P2.8.

2.9 A particular inverting circuit uses an ideal op amp and two 10-kΩ resistors. What closed-loop gain would you expect? If a dc voltage of +1.00 V is applied at the input, what outputs result? If the 10-kΩ resistors are said to be "1% resistors," having values somewhere in the range (1 ± 0.01) times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 1.00 V?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

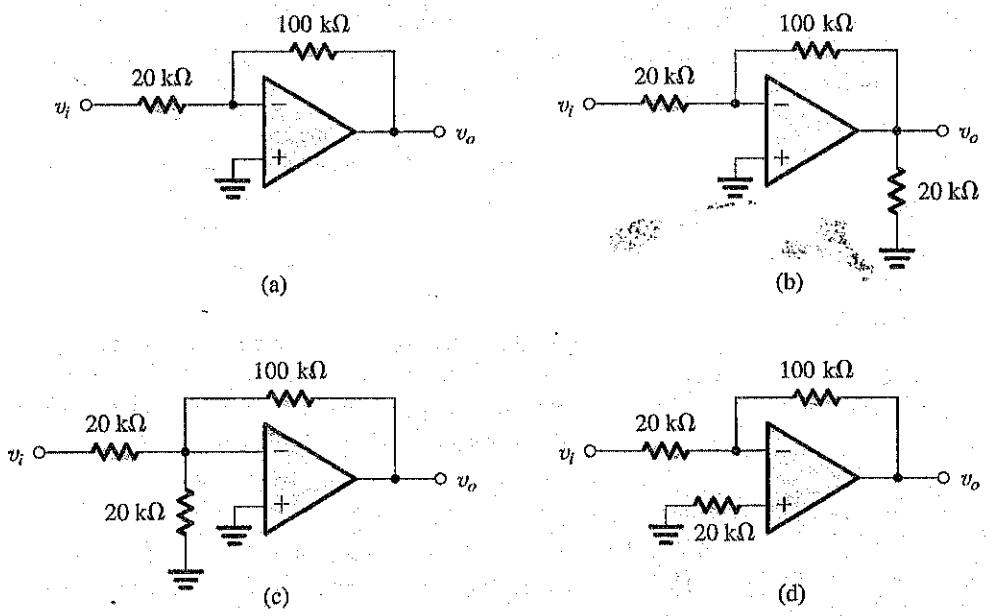

Figure P2.8

2.10 You are provided with an ideal op amp and three 10-kΩ resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage gain magnitude? What is the smallest (nonzero) available gain magnitude? What are the input resistances in these two cases?

SIM 2.11 For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

(a) $R_1 = 10\ \text{k}\Omega, R_2 = 10\ \text{k}\Omega$
(b) $R_1 = 10\ \text{k}\Omega, R_2 = 100\ \text{k}\Omega$
(c) $R_1 = 10\ \text{k}\Omega, R_2 = 1\ \text{k}\Omega$
(d) $R_1 = 100\ \text{k}\Omega, R_2 = 10\ \text{M}\Omega$
(e) $R_1 = 100\ \text{k}\Omega, R_2 = 1\ \text{M}\Omega$

D 2.12 Given an ideal op amp, what are the values of the resistors R_1 and R_2 to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one 10-kΩ resistor and another equal or larger resistor.

(a) −1 V/V
(b) −2 V/V
(c) −5 V/V
(d) −100 V/V

D 2.13 Design an inverting op-amp circuit for which the gain is −10 V/V and the total resistance used is 110 kΩ.

D 2.14 Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of 46 dB having the largest possible input resistance under the constraint of having to use resistors no larger than 1 MΩ. What is the input resistance of your design?

2.15 An ideal op amp is connected as shown in Fig. 2.5 with $R_1 = 10\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$. A symmetrical square-wave signal with levels of 0 V and −1 V is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

2.16 For the circuit in Fig. P2.16, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(b) Find the currents I_1, I_2, I_3, and I_4, in terms of the input current I.
(c) Find the voltages at nodes 1, 2, 3, and 4, that is, V_1, V_2, V_3, and V_4 in terms of (IR).

2.32 The circuit in Fig. P2.32 utilizes an ideal op amp.

(a) Find I_1, I_2, I_3, I_L, and V_x.
(b) If V_O is not to be lower than -13 V, find the maximum allowed value for R_L.
(c) If R_L is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in I_L and in V_O?

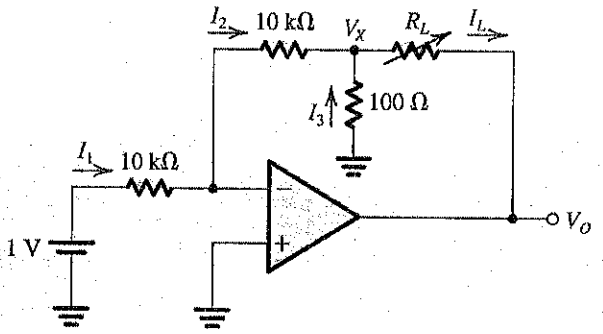

Figure P2.32

D 2.33 Use the circuit in Fig. P2.32 as an inspiration to design a circuit that supplies a constant current I_L of 3.1 mA to a variable resistance R_L. Assume the availability of a 1.5-V battery and design so that the current drawn from the battery is 0.1 mA. For the smallest resistance in the circuit, use 500 Ω. If the op amp saturates at ±10 V, what is the maximum value that R_L can have while the current source supplying it operates properly?

D 2.34 Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.34 to implement a current amplifier with gain $i_L/i_I = 11$ A/A.

(a) Find the required value for R.
(b) What are the input and the output resistance of this current amplifier?
(c) If $R_L = 1$ kΩ and the op amp operates in an ideal manner as long as v_O is in the range ±12 V, what range of i_I is possible?
(d) If the amplifier is fed with a current source having a current of 0.2 mA and a source resistance of 10 kΩ, find i_L.

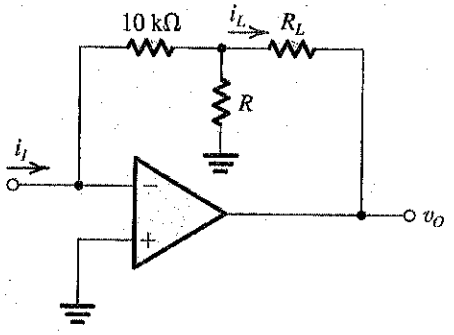

Figure P2.34

D 2.35 Design the circuit shown in Fig. P2.35 to have an input resistance of 100 kΩ and a gain that can be varied from -1 V/V to -100 V/V using the 100-kΩ potentiometer R_4. What voltage gain results when the potentiometer is set exactly at its middle value?

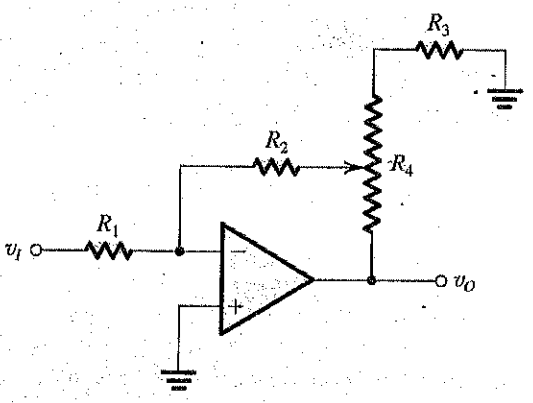

Figure P2.35

2.36 A weighted summer circuit using an ideal op amp has three inputs using 10-kΩ resistors and a feedback resistor of 50 kΩ. A signal v_1 is connected to two of the inputs while a signal v_2 is connected to the third. Express v_O in terms of v_1 and v_2. If $v_1 = 1$ V and $v_2 = -1$ V, what is v_O?

D 2.37 Design an op-amp circuit to provide an output $v_O = -[2v_1 + (v_2/2)]$. Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed 50 μA for 1-V input signals.

D 2.38 Use the scheme illustrated in Fig. 2.10 to design an op-amp circuit with inputs v_1, v_2, and v_3, whose output is

either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

D 2.46 Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage V applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100 μA, find the value of R such that a full-scale reading is obtained when V is +10 V. Does the meter resistance shown affect the voltmeter calibration?

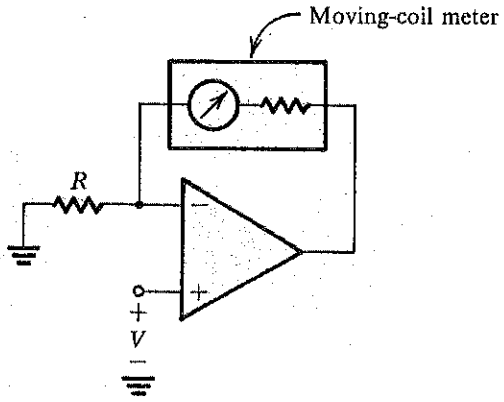

Figure P2.46

D *2.47 (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = \left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_P}{R_{P1}}v_{P1} + \frac{R_P}{R_{P2}}v_{P2} + \cdots + \frac{R_P}{R_{Pn}}v_{Pn}\right]$$

where $R_N = R_{N1} \| R_{N2} \| \cdots \| R_{Nn}$, and

$$R_P = R_{P1} \| R_{P2} \| \cdots \| R_{Pn} \| R_{P0}$$

(b) Design a circuit to obtain

$$v_O = -4v_{N1} + v_{P1} + 3v_{P2}$$

The smallest resistor used should be 10 kΩ.

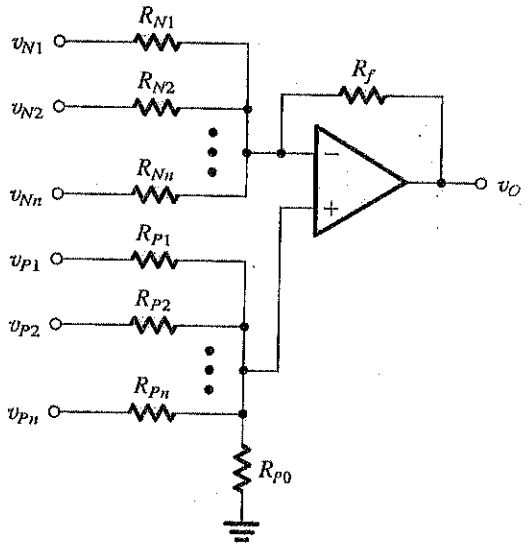

Figure P2.47

D *2.48 Design a circuit, using one ideal op amp, whose output is $v_O = v_{I1} + 2v_{I2} - 9v_{I3} + 4v_{I4}$. (*Hint:* Use a structure similar to that shown in general form in Fig. P2.47.)

2.49 Derive an expression for the voltage gain, v_O/v_I, of the circuit in Fig. P2.49.

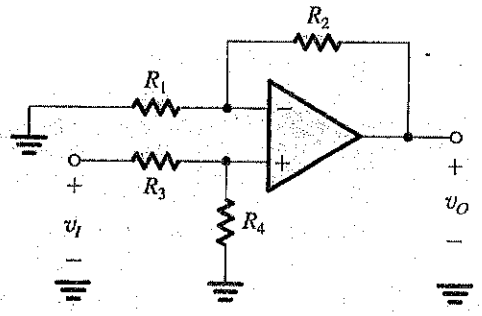

Figure P2.49

2.50 For the circuit in Fig. P2.50, use superposition to find v_O in terms of the input voltages v_1 and v_2. Assume an ideal op amp. For

$$v_1 = 10\sin(2\pi \times 60t) - 0.1\sin(2\pi \times 1000t), \text{ volts}$$
$$v_2 = 10\sin(2\pi \times 60t) + 0.1\sin(2\pi \times 1000t), \text{ volts}$$

find v_O.

where K is the nominal (ideal) value of the ratios (R_2/R_1) and (R_4/R_3). Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used. What resistor tolerance is needed if a CMRR of 80 dB is required?

D *2.67 Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 1000, a differential input resistance of 2 kΩ, and a minimum CMRR of 88 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than x%).

***2.68** (a) Find A_d and A_{cm} for the difference amplifier circuit shown in Fig. P2.68.

(b) If the op amp is specified to operate properly as long as the common-mode voltage at its positive and negative inputs falls in the range ±2.5 V, what is the corresponding limitation on the range of the input common-mode signal v_{icm}? (This is known as the **common-mode range** of the differential amplifier.)

(c) The circuit is modified by connecting a 10-kΩ resistor between node A and ground, and another 10-kΩ resistor between node B and ground. What will now be the values of A_d, A_{cm}, and the input common-mode range?

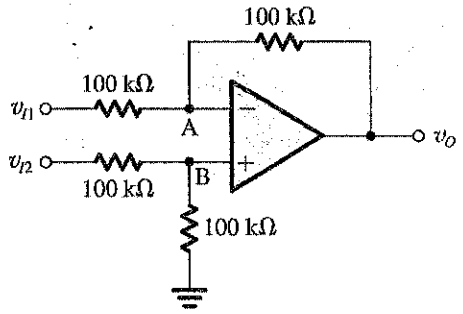

Figure P2.68

D *2.69 To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor R connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5, R_6) connected across the output feeds a fraction β of the output, that is, a voltage βv_O, back to the positive-input terminal of the op amp through a resistor R. Assume that R_5 and R_6 are much smaller than R so that the current through R is much lower than the current in the voltage divider, with the result that $\beta \simeq R_6/(R_5 + R_6)$. Show that the differential gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{1}{1-\beta}$$

(*Hint:* Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of 2 MΩ. Select values for R, R_5, and R_6, such that $(R_5 + R_6) \ll R/100$.

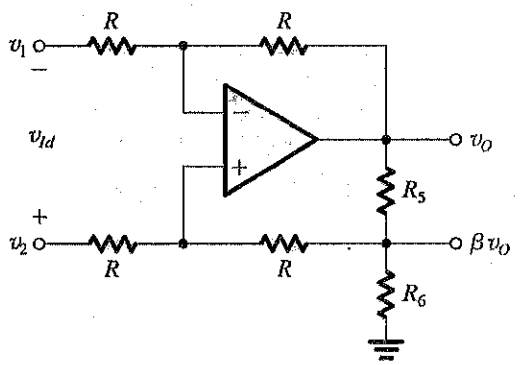

Figure P2.69

***2.70** Figure P2.70 shows a modified version of the difference amplifier. The modified circuit includes a resistor R_G, which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_O}{v_{Id}} = -2\frac{R_2}{R_1}\left[1 + \frac{R_2}{R_G}\right]$$

(*Hint:* The virtual short circuit at the op-amp input causes the current through the R_1 resistors to be $v_{Id}/2R_1$).

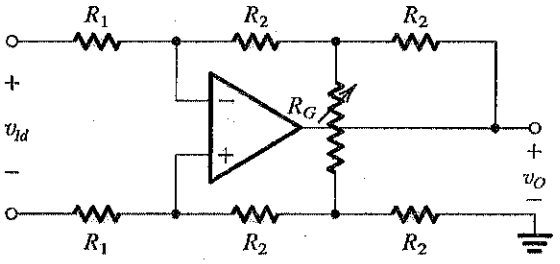

Figure P2.70

MULTISIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch v_O.
(b) What is the voltage gain v_O/v_I?
(c) Assuming that the op amps operate from ±15-V power supplies and that their output saturates at ±14 V (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

*2.78 The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance Z_L with a current proportional to v_I and independent of the value of Z_L. Show that this is indeed the case, and find for each circuit i_O as a function of v_I. Comment on the differences between the two circuits.

Section 2.5: Integrators and Differentiators

2.79 A Miller integrator incorporates an ideal op amp, a resistor R of 10 kΩ, and a capacitor C of 1 nF. A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?
(b) At that frequency, how does the phase of the output sine wave relate to that of the input?
(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?
(d) What is the phase relation between the input and output in situation (c)?

D 2.80 Design a Miller integrator with a time constant of 1 s and an input resistance of 100 kΩ. A dc voltage of −1 volt is applied at the input at time 0, at which moment $v_O = -10$ V. How long does it take the output to reach 0 V? +10 V?

2.81 An op-amp-based inverting integrator is measured at 10 kHz to have a voltage gain of −100 V/V. At what frequency is its gain reduced to −1 V/V? What is the integrator time constant?

D 2.82 Design a Miller integrator that has a unity-gain frequency of 10 krad/s and an input resistance of 100 kΩ. Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V, 100-μs pulse is applied to the input. Characterize the output that results when a sine wave 2 sin $10^4 t$ is applied to the input.

D 2.83 Design a Miller integrator whose input resistance is 10 kΩ and unity-gain frequency is 100 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor to limit the dc gain

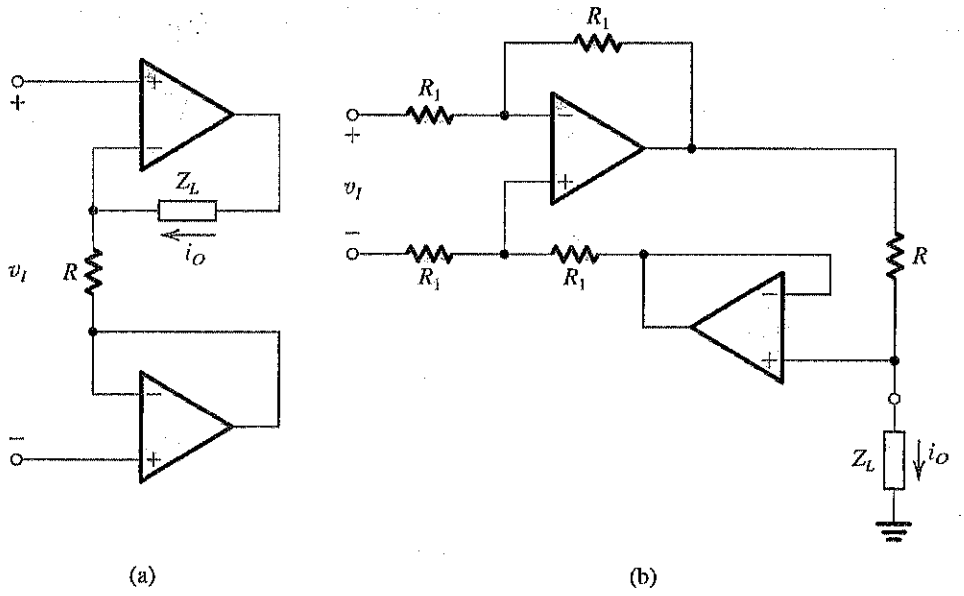

Figure P2.78

= Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem