model of Fig. 7.26(b). Show that

$$R_{\text{in}} \equiv \frac{v_i}{i_b} = (\beta + 1)(r_e + R_e)$$

$$\frac{v_o}{v_i} = \frac{R_e}{R_e + r_e}$$

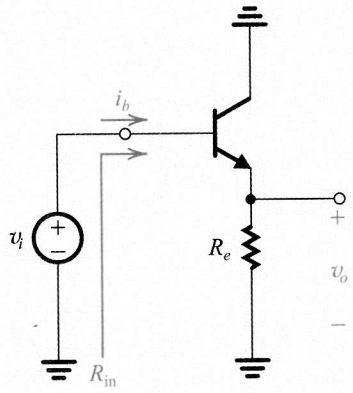

Figure P7.52

7.53 For the circuit shown in Fig. P7.53, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use $\alpha = 0.99$). Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in}? Calculate the overall voltage gain (v_o/v_{sig}).

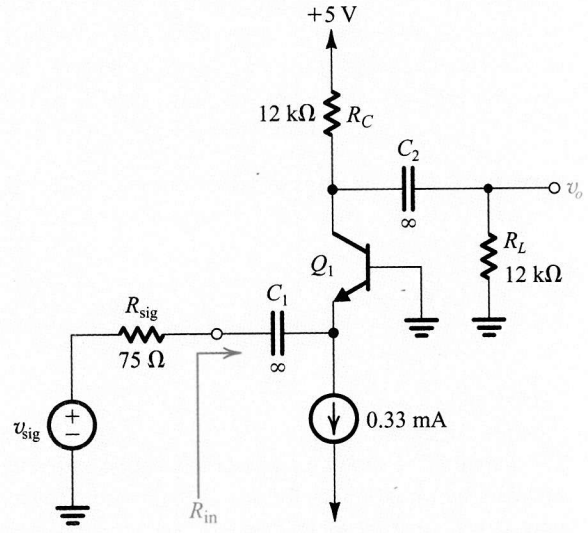

Figure P7.53

7.54 In the circuit shown in Fig. P7.54, the transistor has a β of 200. What is the dc voltage at the collector? Replacing the BJT with one of the hybrid-π models (neglecting r_o), draw the equivalent circuit of the amplifier. Find the input resistances R_{ib} and R_{in} and the overall voltage gain (v_o/v_{sig}). For an output signal of ±0.4 V, what values of v_{sig} and v_b are required?

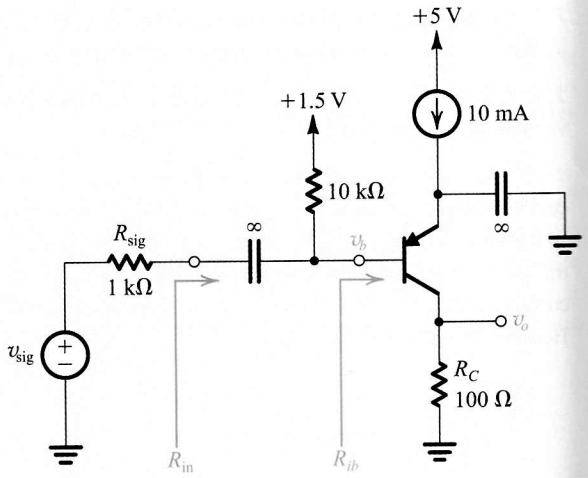

Figure P7.54

7.55 Consider the augmented hybrid-π model shown in Fig. 7.25(a). Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for $V_A = 25$ V and $V_A = 125$ V.

D 7.56 Redesign the circuit of Fig. 7.30(a) by raising the resistor values by a factor n to increase the resistance seen by the input v_i to 75 Ω. What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be "matched" to the equivalent resistances of the interconnecting cables.

D *7.57 Design an amplifier using the configuration of Fig. 7.30(a). The power supplies available are ±5 V. The input signal source has a resistance of 50 Ω, and it is required that the amplifier input resistance match this value. (Note that $R_{\text{in}} = r_e \| R_E \simeq r_e$.) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base–emitter junction should be limited to no more

This feedback amplifier circuit and the gain formula should remind you of an op amp connected in the noninverting configuration. We shall study feedback formally in Chapter 11.

7.125 For the common-emitter amplifier shown in Fig. P7.125, let $V_{CC} = 15$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 2.4$ kΩ, and $R_C = 3.9$ kΩ. The transistor has $\beta = 100$. Calculate the dc bias current I_C. If the amplifier operates between a source for which $R_{sig} = 2$ kΩ and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, and the overall voltage gain v_o/v_{sig}.

D 7.126 Using the topology of Fig. P7.125, design an amplifier to operate between a 2-kΩ source and a 2-kΩ load with a gain v_o/v_{sig} of –40 V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has $\beta = 100$. Use standard 5% resistors (see Appendix J).

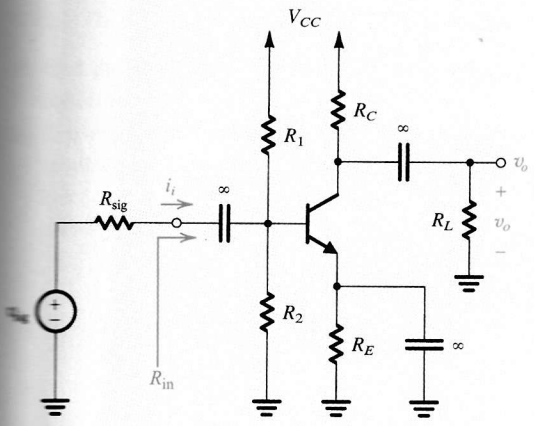

Figure P7.125

D 7.127 A designer, having examined the situation described in Problem 7.125 and estimating the available gain to be approximately –36.3 V/V, wants to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 7.2 kΩ, and R_C to 12 kΩ (standard values of 5%-tolerance resistors). With $V_{CC} = 15$ V, $R_{sig} = 2$ kΩ, $R_L = 2$ kΩ, and $\beta = 100$, what does the gain become? Comment.

D 7.128 The CE amplifier circuit of Fig. P7.128 is biased with a constant-current source I. It is required to design the circuit (i.e., find values for I, R_B, and R_C) to meet the following specifications:

(a) $R_{in} \simeq 10$ kΩ.
(b) The dc voltage drop across R_B is approximately 0.2 V.
(c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that v_{sig} is a sinusoidal source, the available supply $V_{CC} = 5$ V, and the transistor has $\beta = 100$. Use standard 5% resistance values, and specify the value of I to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If $R_{sig} = R_L = 20$ kΩ, what is the overall voltage gain?

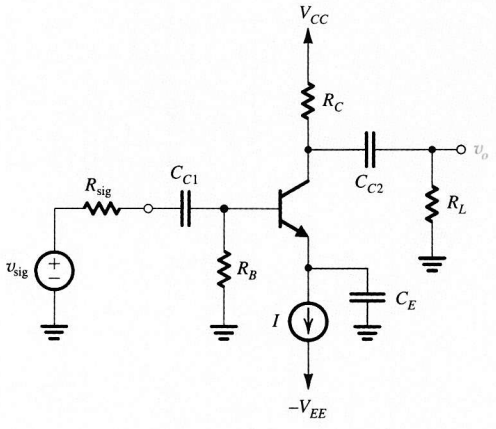

Figure P7.128

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.131 In the circuit of Fig. P7.131, the BJT is biased with a constant-current source, and v_{sig} is a small sine-wave signal. Find R_{in} and the gain v_o/v_{sig}. Assume $\beta = 100$. If the amplitude of the signal v_{be} is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

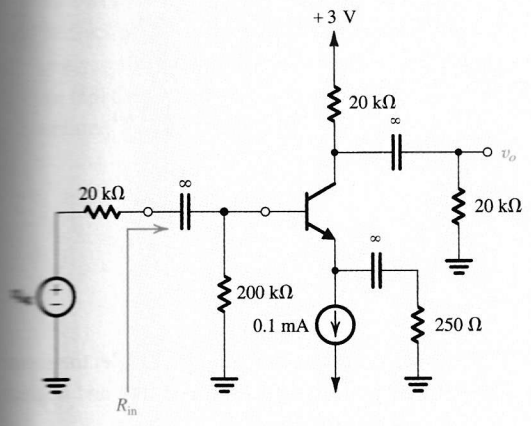

Figure P7.131

***7.132** The BJT in the circuit of Fig. P7.132 has $\beta = 100$.

(a) Find the dc collector current and the dc voltage at the collector.

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

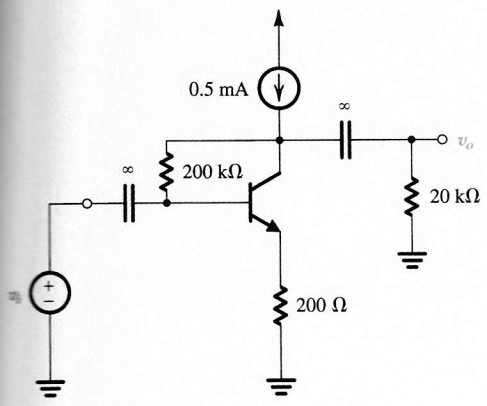

Figure P7.132

7.133 For the circuit in Fig. P7.133, find the input resistance R_{in} and the voltage gain v_o/v_{sig}. Assume that the source provides a small signal v_{sig} and that $\beta = 100$.

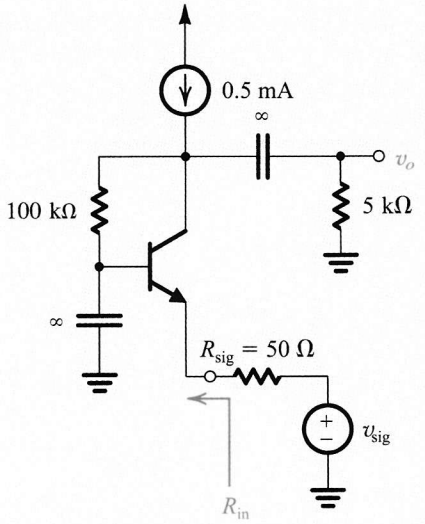

Figure P7.133

7.134 For the emitter-follower circuit shown in Fig. P7.134, the BJT used is specified to have β values in the range of 50 to 200 (a distressing situation for the circuit designer).

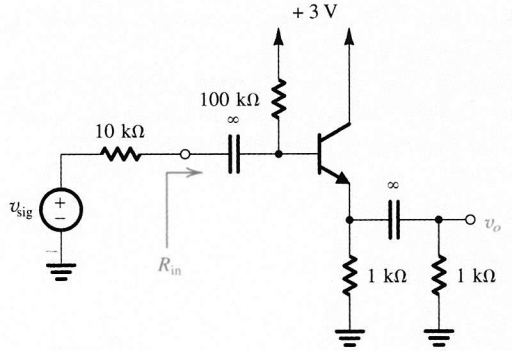

Figure P7.134

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem