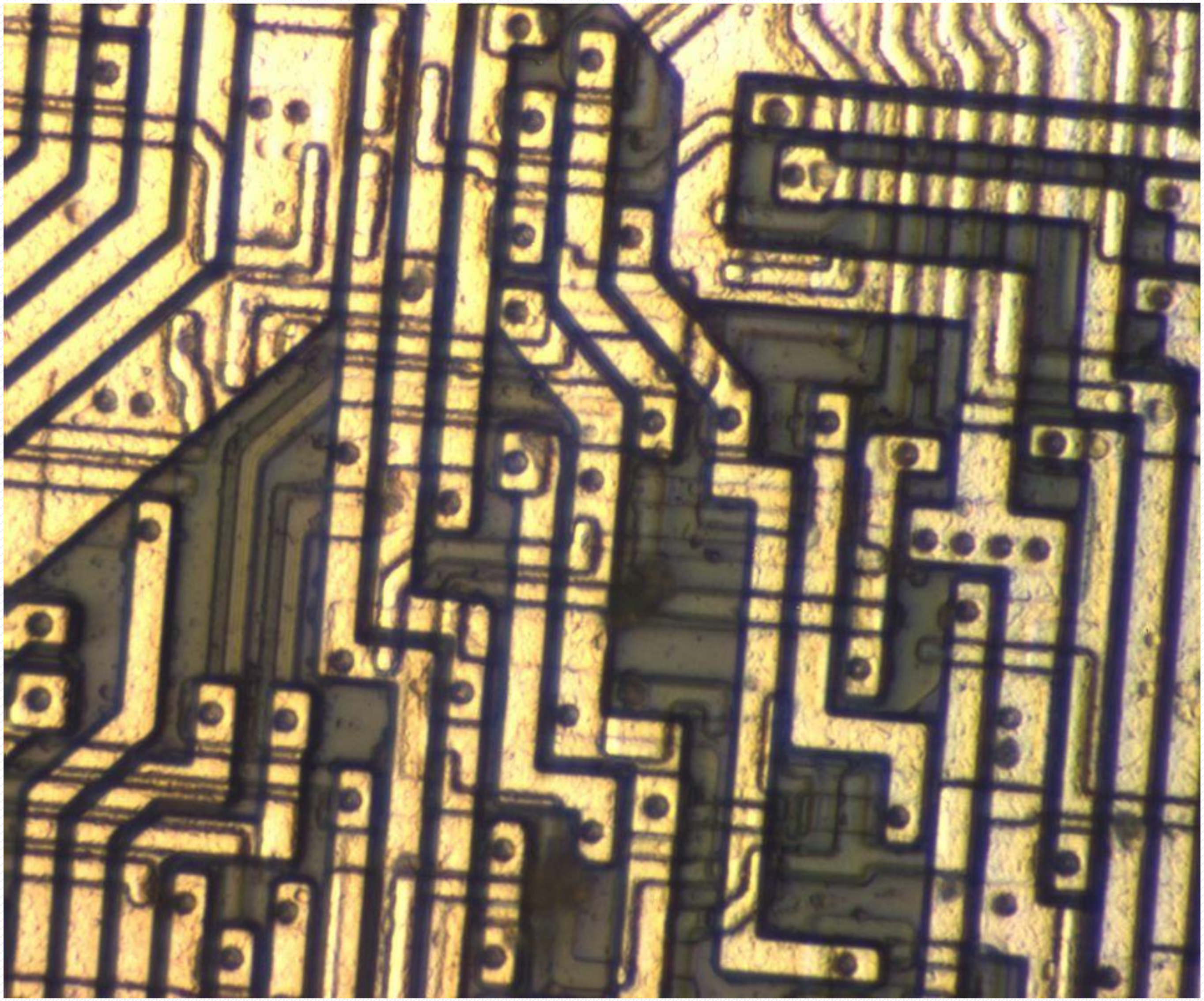
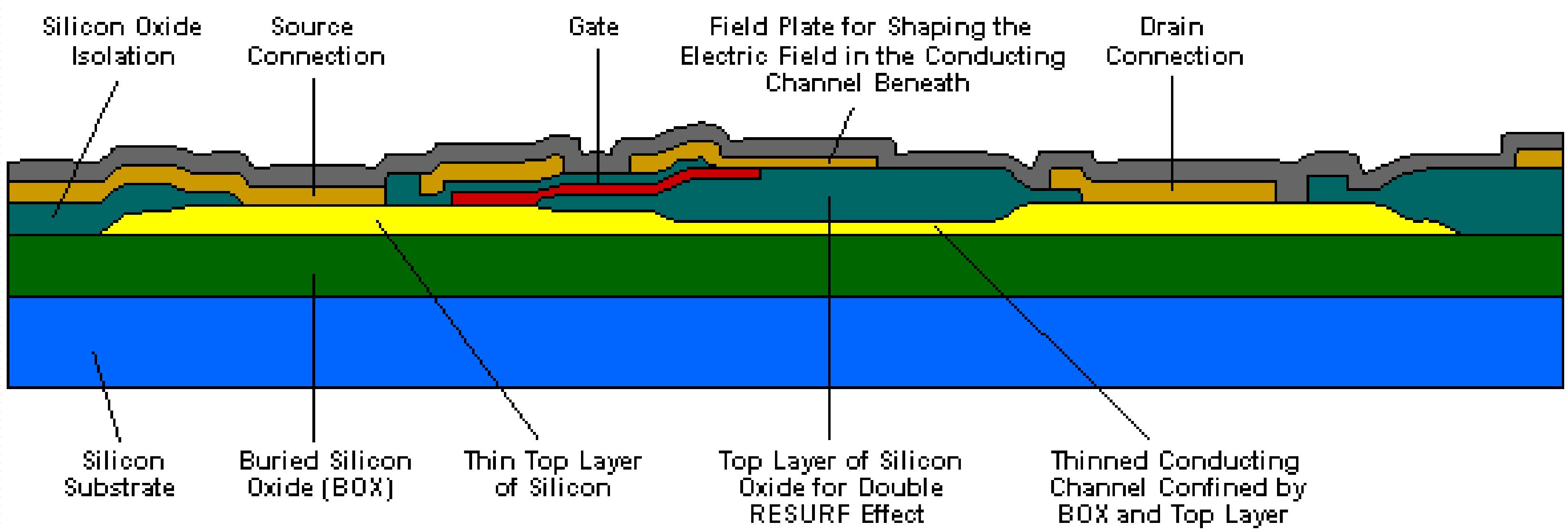
Junction – Part 1

Outline

- **Introduction**
- **Theory and concept of junction**
- **Technology of junction**
- **Types of junction in devices**



Example: Cross section



Introduction

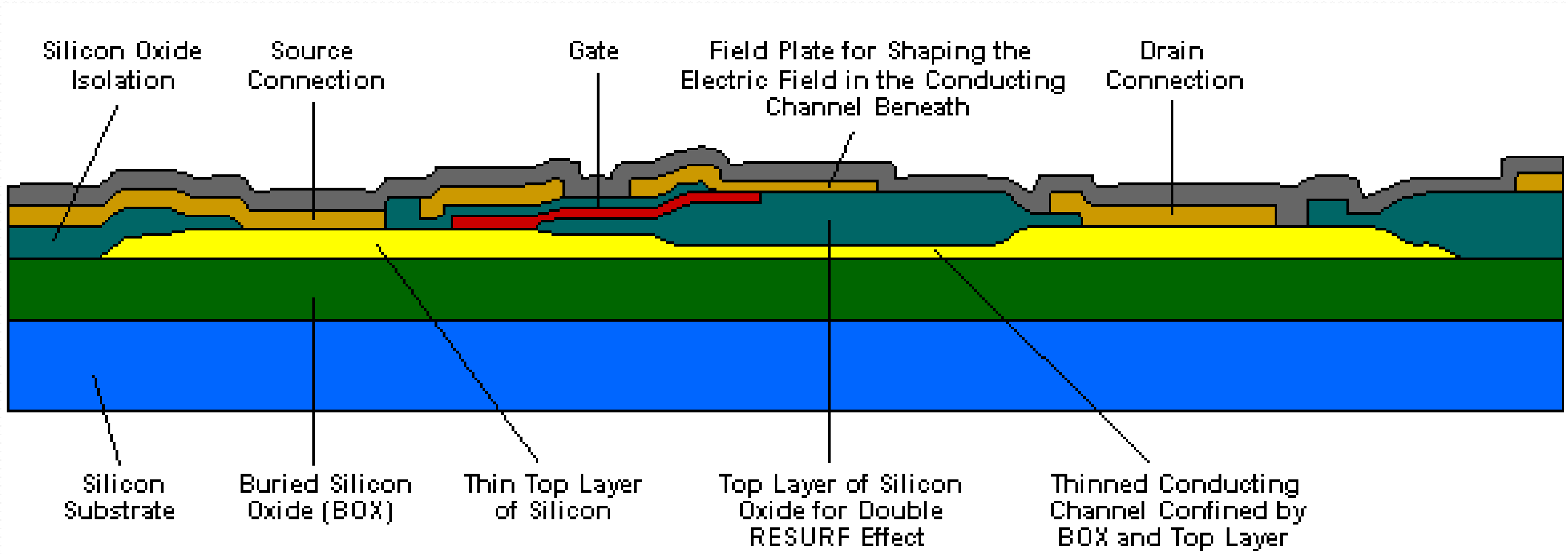
- **What is a junction?**

  A boundary region between domains with dissimilar electronic characteristics. Examples: p-n junction in diodes and transistors, heterojunction between different semiconductors, insulator-metal or insulator-semiconductor junctions, Ohmic and Schottky metal-semiconductor junctions

- **Why junctions?**

  A device without any junctions is a piece of material with uniform characteristic throughout. What do you think its electrical behavior is like? e. g. I-V curve? <u>what can we do with it?</u>

Example: Cross section



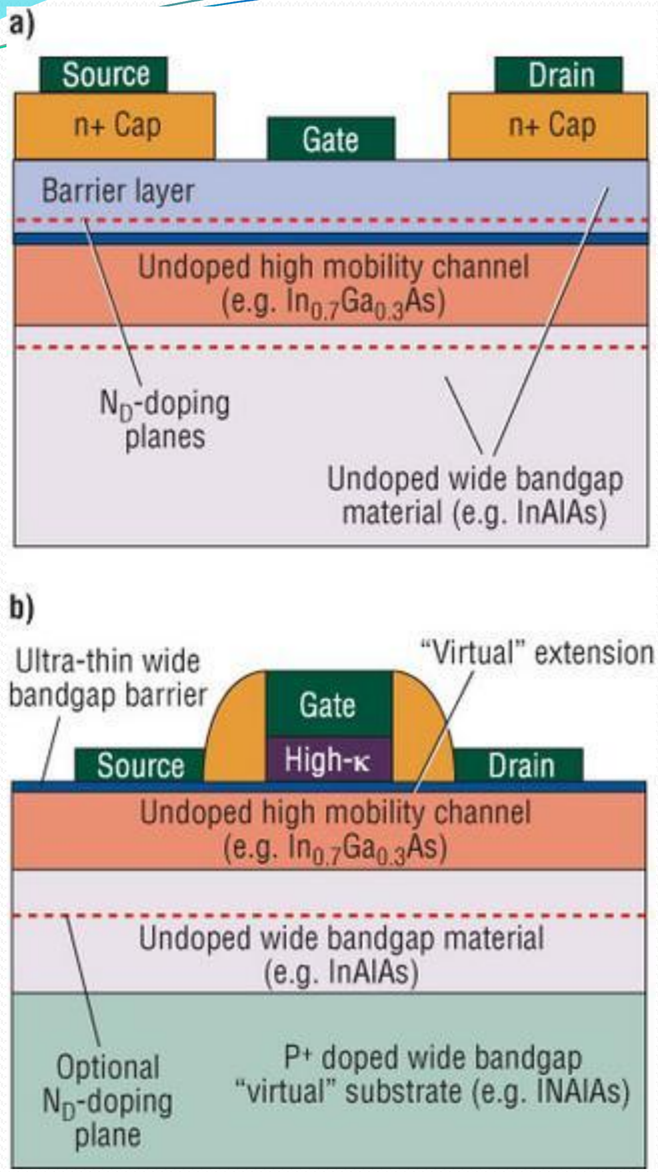
How to make junctions

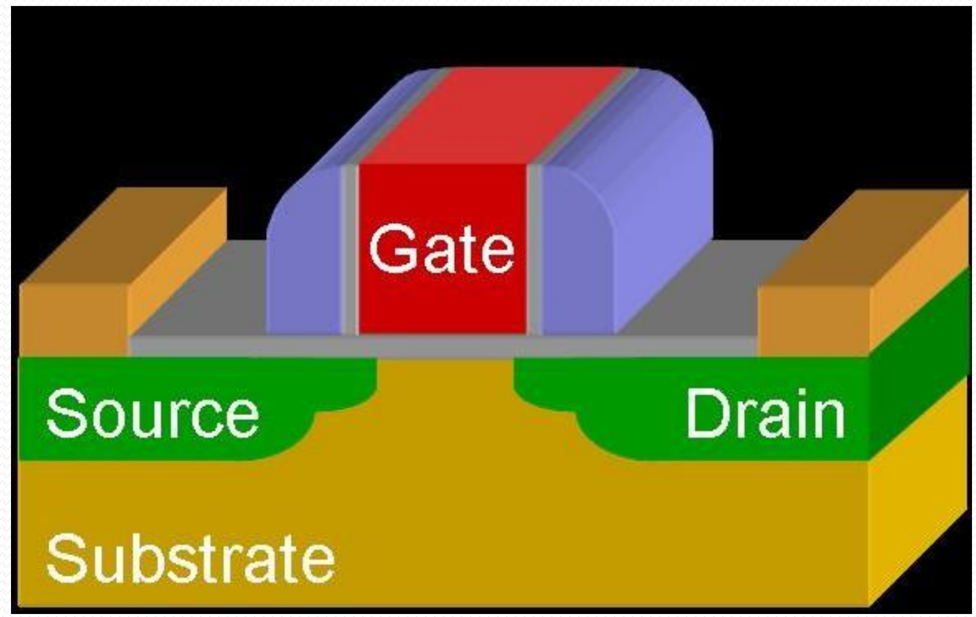
- Put 2 dissimilar domains together: deposition, epitaxial growth
- Induce a change in a small domain within a larger domain. The change can be: carrier types, carrier concentration and/or spatial profile. Alloying, diffusion, ion implantation.
- Making junctions is almost the same as making devices. Extensive R&D have been devoted to the fabrication technology. Many problems have been solved, but from time to time, still new progress, breakthru

http://www.youtube.com/watch?v=TXvhyvwttRE

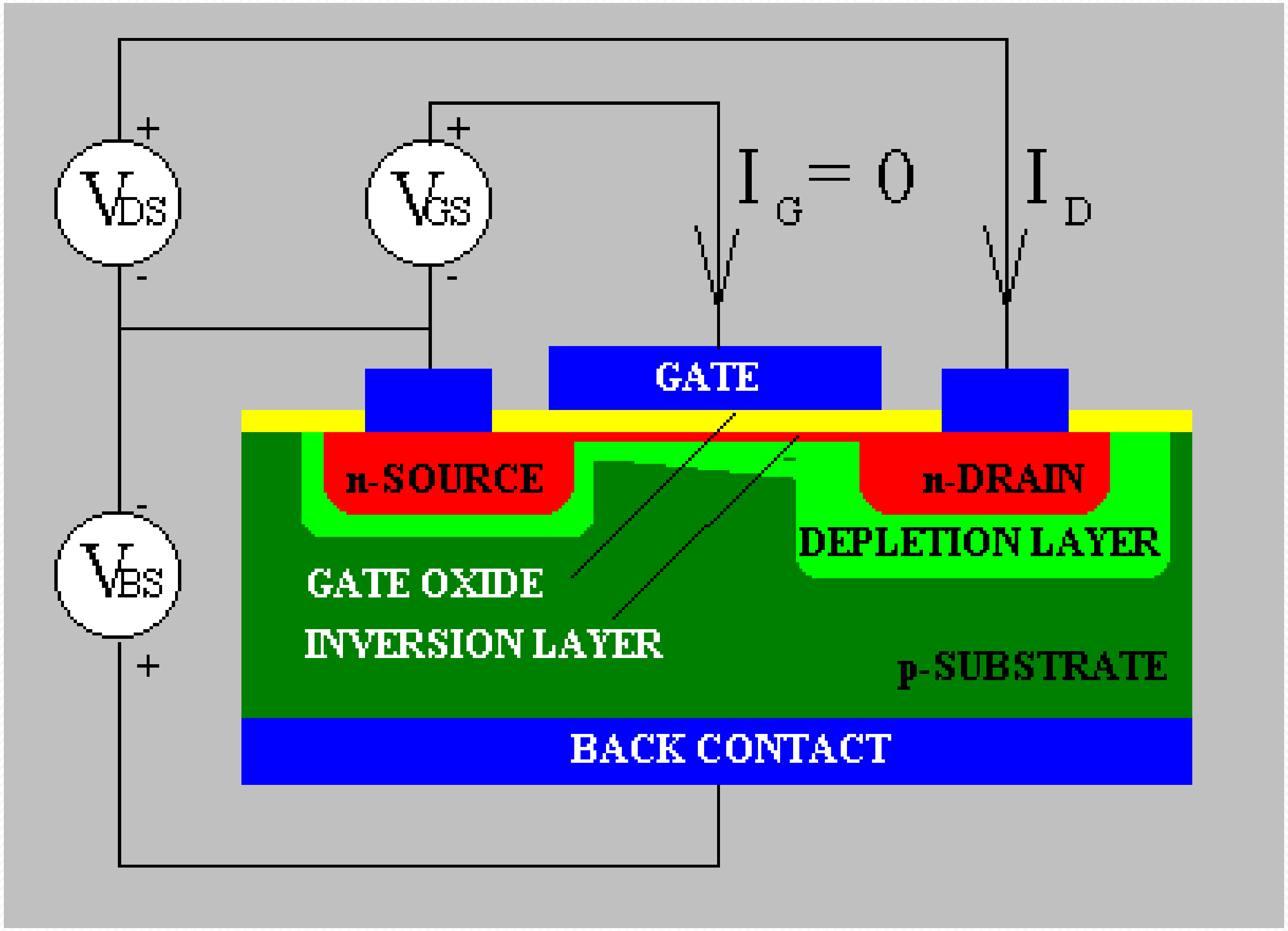
What about junctions?

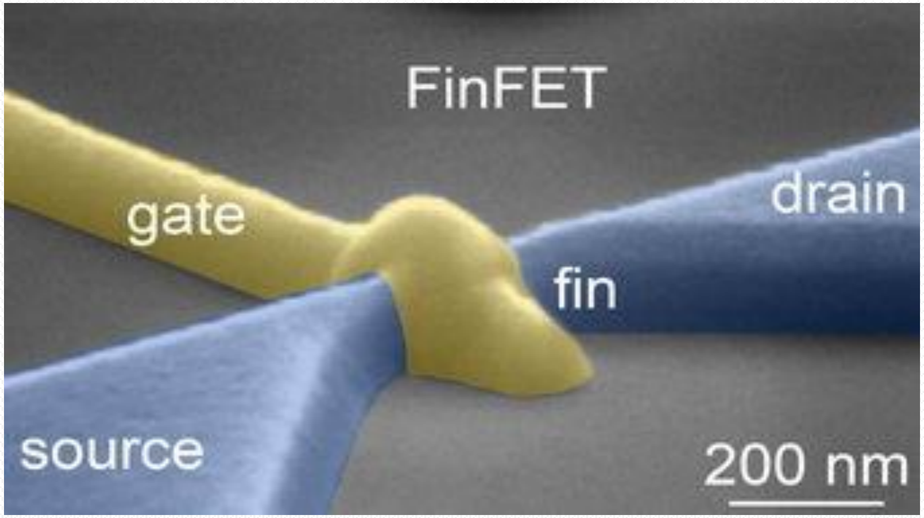
- How does it work?
- How does a junction behave in an electrical circuit? Is it like an R, C, L, or a vacuum diode? How do we describe its properties? If a junction behaves like an R, C, or L, is there any reason for us to be so interested in them?
- How is it applied?
- **Junction is the key building block of solid state devices:**
  - Fundamental physics
  - Material and fabrication technology
  - Device design

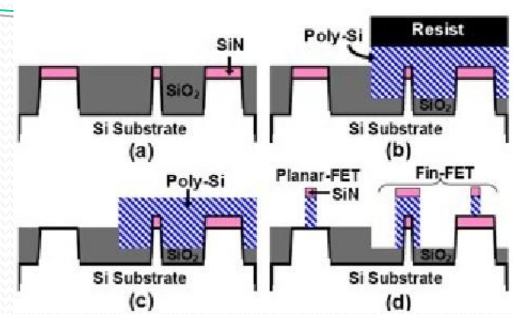

a)
Source
Drain
n+ Cap
Gate
n+ Cap
Barrier layer
Undoped high mobility channel
(e.g. $In_{0.7}Ga_{0.3}As$)
N_D-doping
planes
Undoped wide bandgap
material (e.g. InAlAs)
b)
Ultra-thin wide
bandgap barrier
"Virtual" extension
Gate
High-κ
Source
Drain
Undoped high mobility channel
(e.g. $In_{0.7}Ga_{0.3}As$)
Undoped wide bandgap material
(e.g. InAlAs)
Optional
N_D-doping
plane
P+ doped wide bandgap
"virtual" substrate (e.g. INAlAs)

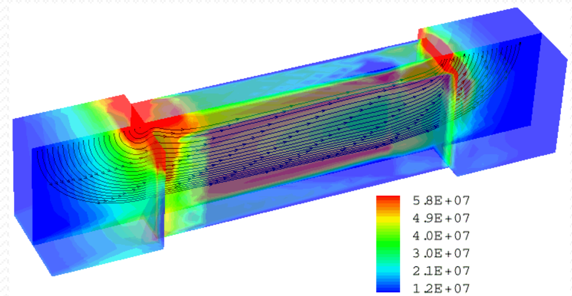

Gate
Source
Drain
Substrate

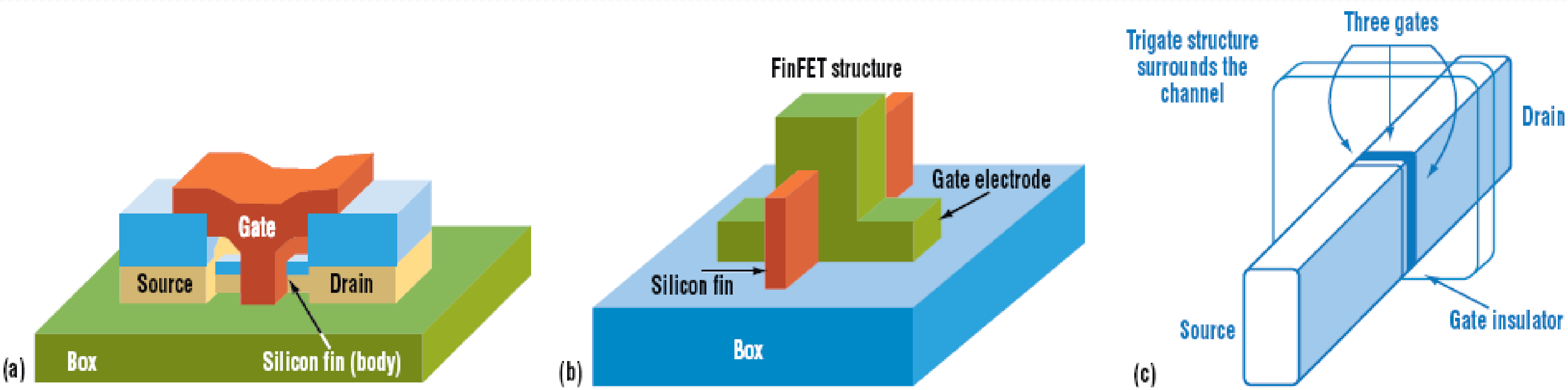
Example: FET
Field Effect Transistor



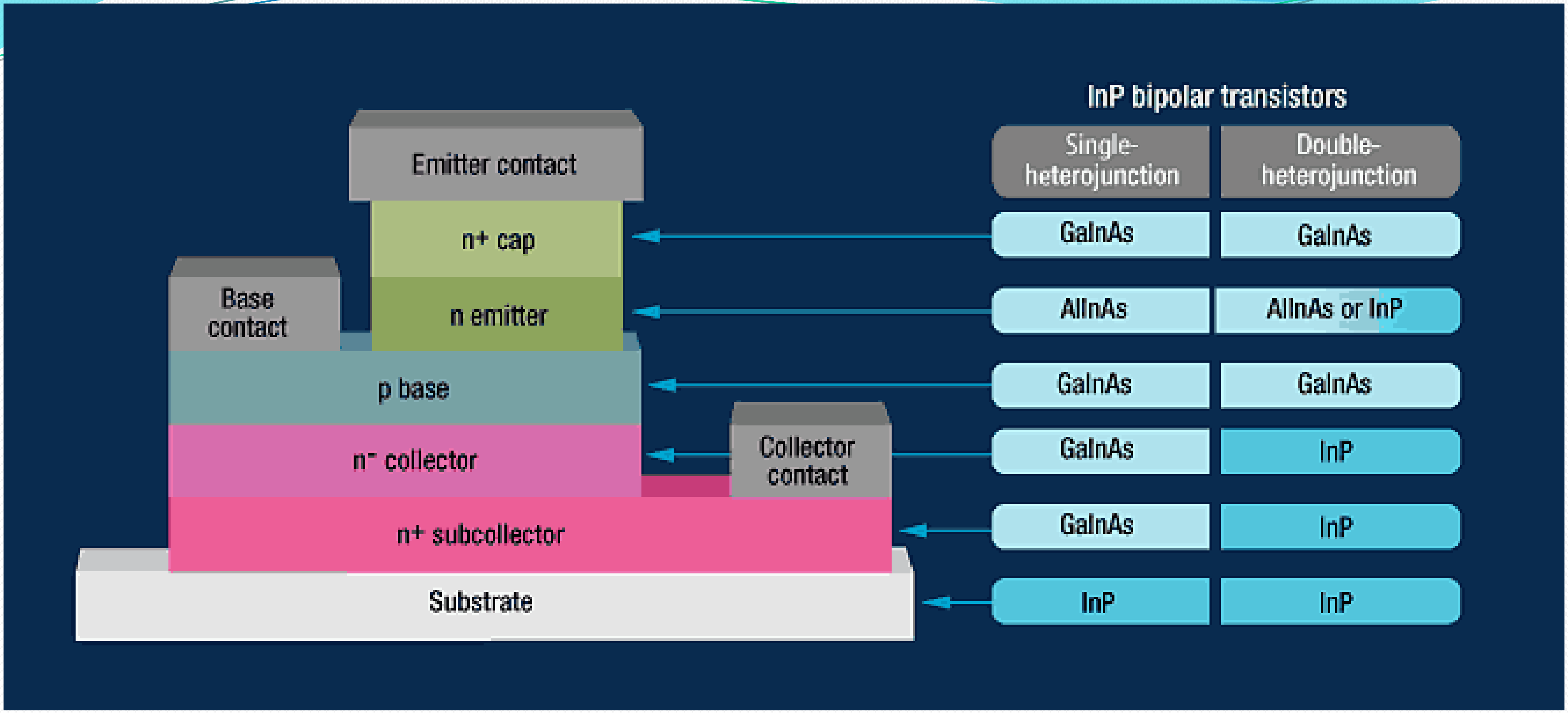




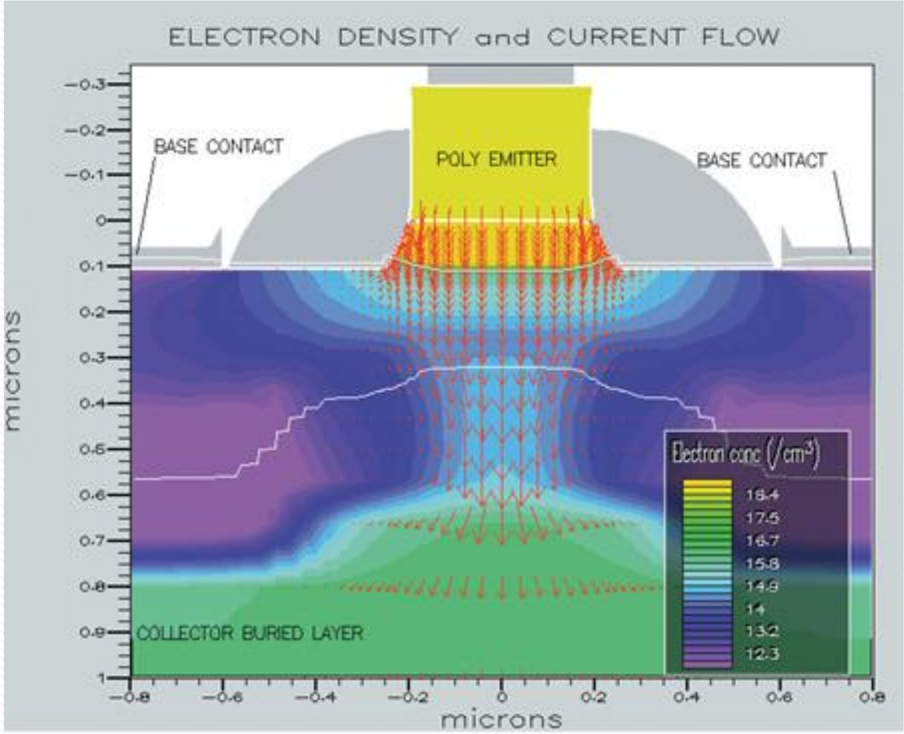


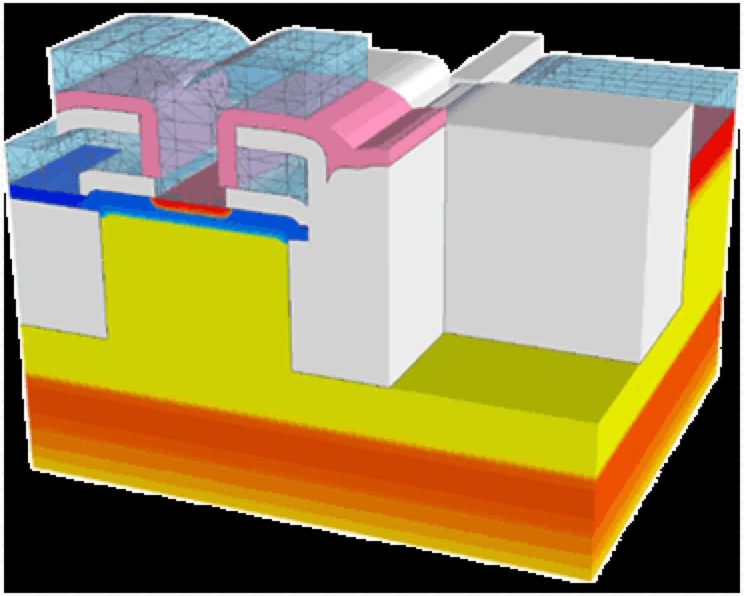


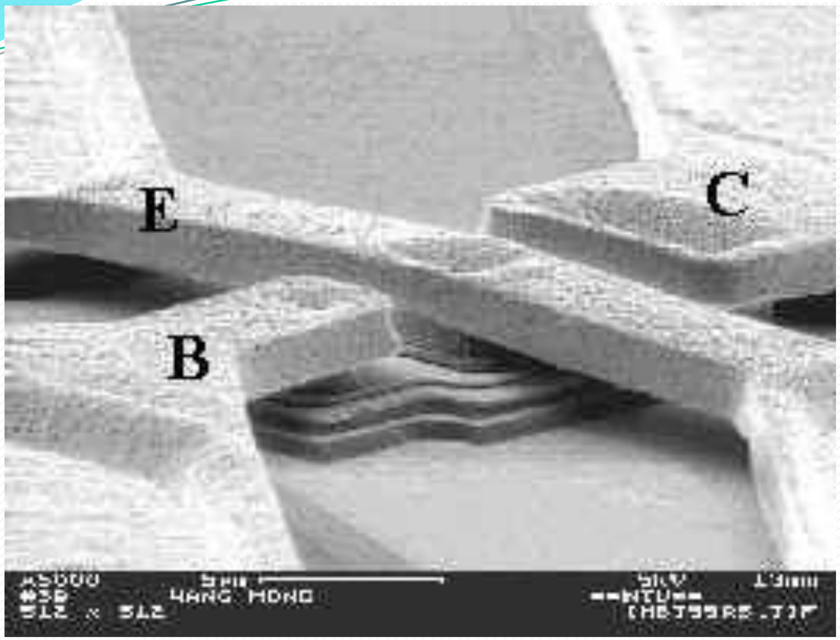
4. A 3D FinFET transistor is composed of a thin silicon film, shown here with a double-gate structure (a and b) and Intel's trigate structure (c).

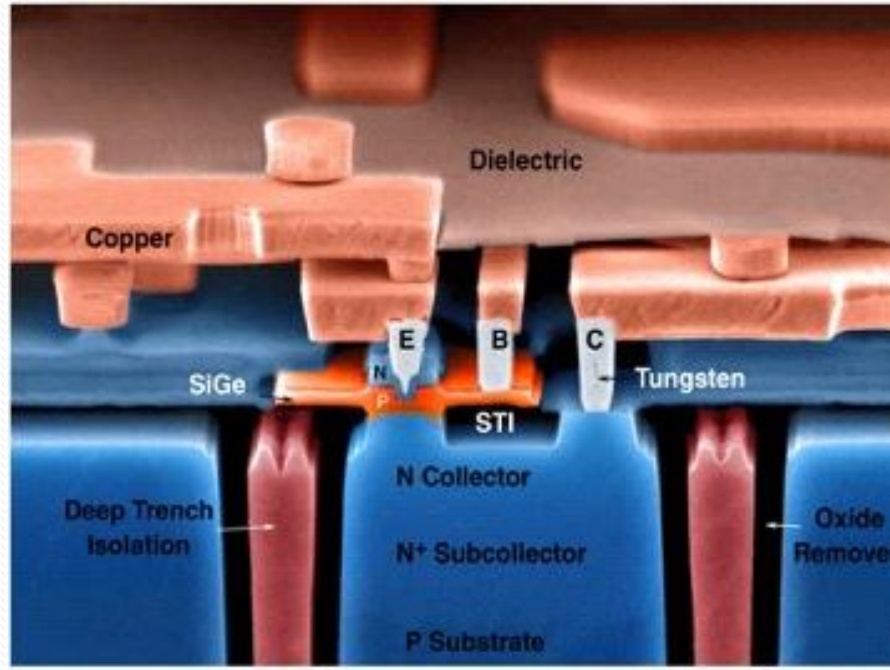


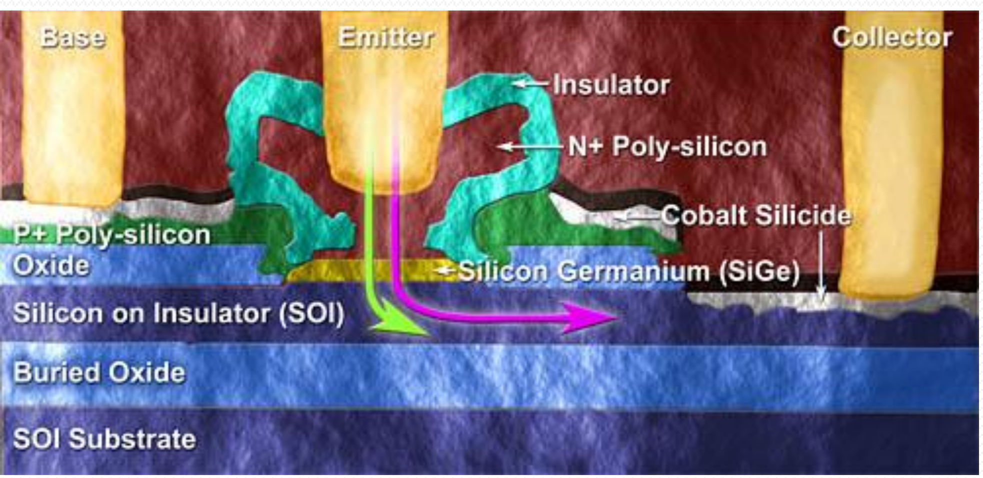
InP bipolar transistors
Emitter contact
n+ cap
Base contact
n emitter
p base
n⁻ collector
Collector contact
n+ subcollector
Substrate
Single-heterojunction
Double-heterojunction
GaInAs
GaInAs
AlInAs
AlInAs or InP
GaInAs
GaInAs
GaInAs
InP
GaInAs
InP
InP
InP

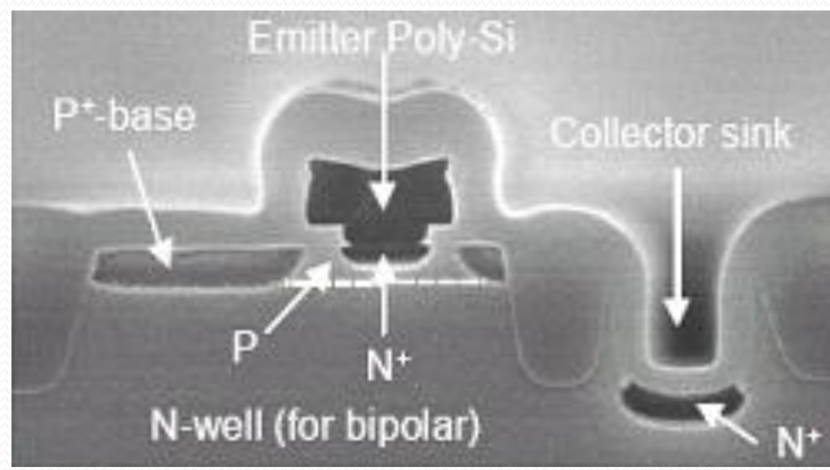

ELECTRON DENSITY and CURRENT FLOW
BASE CONTACT
POLY EMITTER
BASE CONTACT
COLLECTOR BURIED LAYER
Electron conc (/cm3)
18.4
17.5
16.7
15.8
14.9
14
13.2
12.3
microns
microns




E
C
B


Dielectric
Copper
E
B
C
N
P
SiGe
Tungsten
STI
N Collector
Deep Trench
Isolation
Oxide
Removed
N+ Subcollector
P Substrate

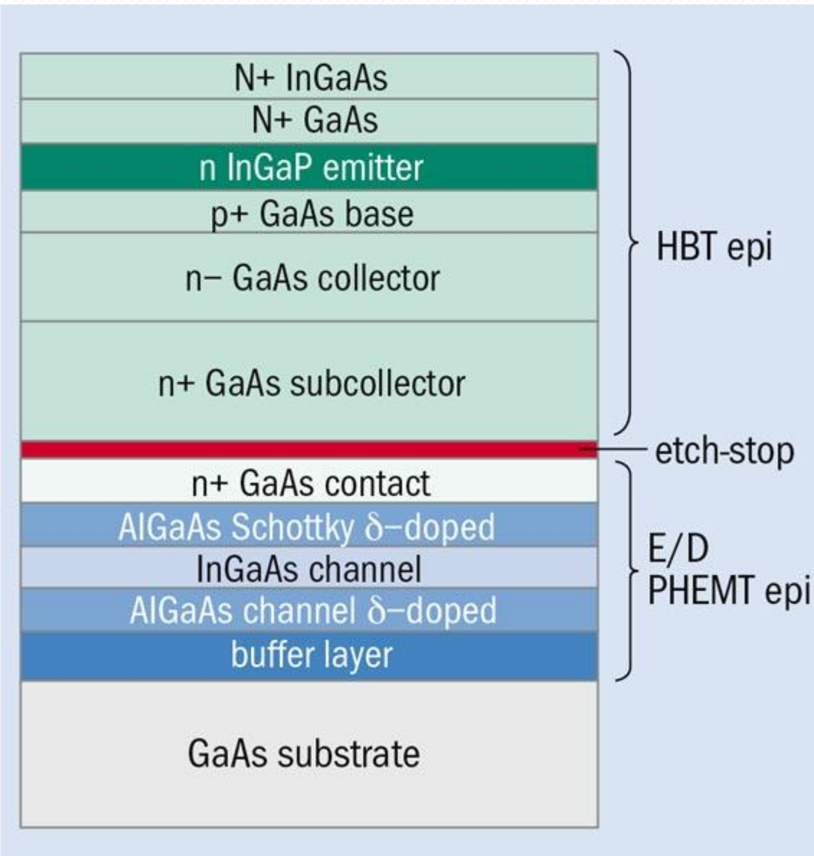

Base
Emitter
Collector
Insulator
N+ Poly-silicon
Cobalt Silicide
P+ Poly-silicon
Oxide
Silicon Germanium (SiGe)
Silicon on Insulator (SOI)
Buried Oxide
SOI Substrate

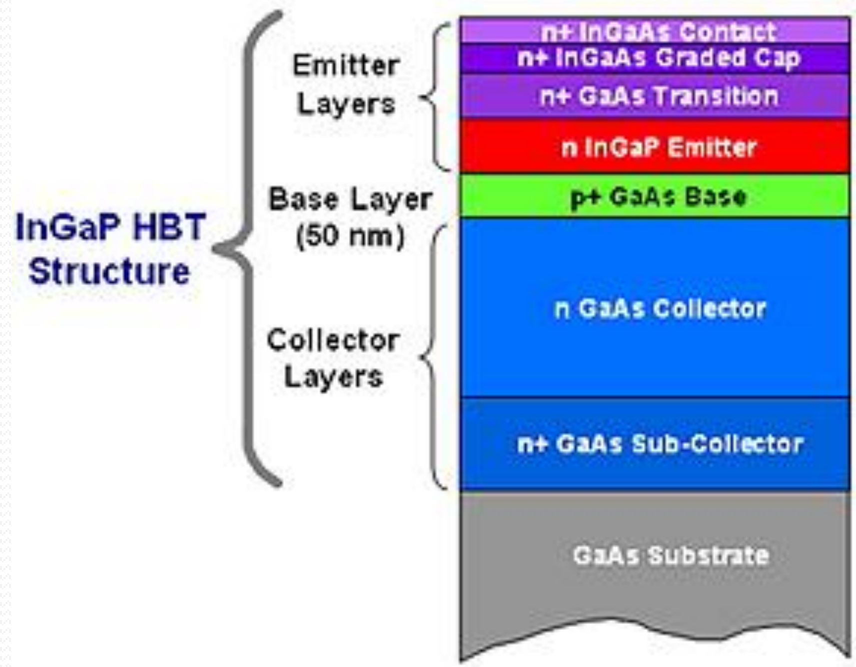

Emitter Poly-Si
P+-base
Collector sink
P
N+
N-well (for bipolar)
N+

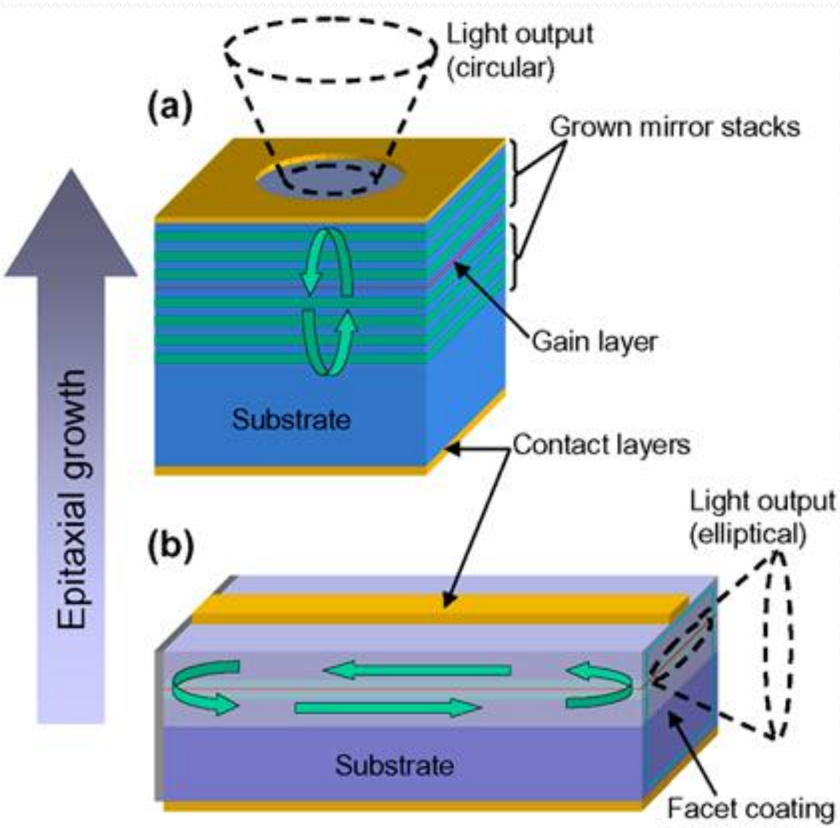
Approaches to study junction

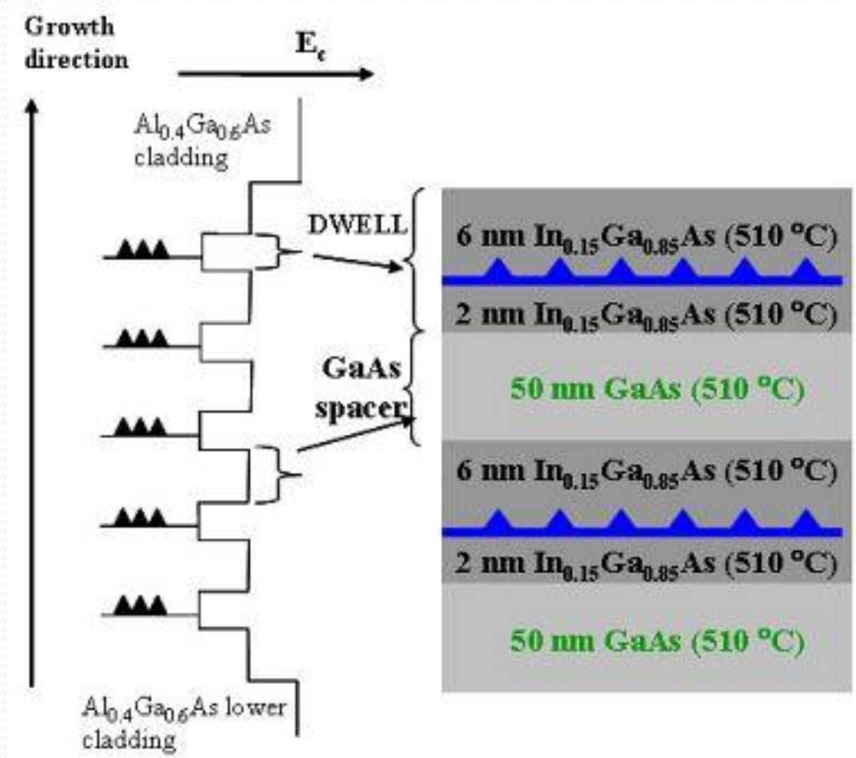
- Types of junctions
- Homogenous semiconductors: same-chemical composition semiconductors; e. g. Si p-n junction
- Heterogenous semiconductors (also called heterojunctions): different alloys, chemical compositions
- Semiconductor-dielectric insulator (e. g. FET)
- Semiconductor-metal: ohmic and Schottky.
- Physical junctions vs. idealized junctions: modeling
- Approximations for various regimes

Heterostructures






Light output
(circular)
(a)
Grown mirror stacks
Gain layer
Substrate
Contact layers
Epitaxial growth
(b)
Light output
(elliptical)
Substrate
Facet coating


Growth
direction
E_c
$Al_{0.4}Ga_{0.6}As$
cladding
DWELL
GaAs
spacer
$Al_{0.4}Ga_{0.6}As$ lower
cladding
6 nm $In_{0.15}Ga_{0.85}As$ (510 °C)
2 nm $In_{0.15}Ga_{0.85}As$ (510 °C)
50 nm GaAs (510 °C)
6 nm $In_{0.15}Ga_{0.85}As$ (510 °C)
2 nm $In_{0.15}Ga_{0.85}As$ (510 °C)
50 nm GaAs (510 °C)

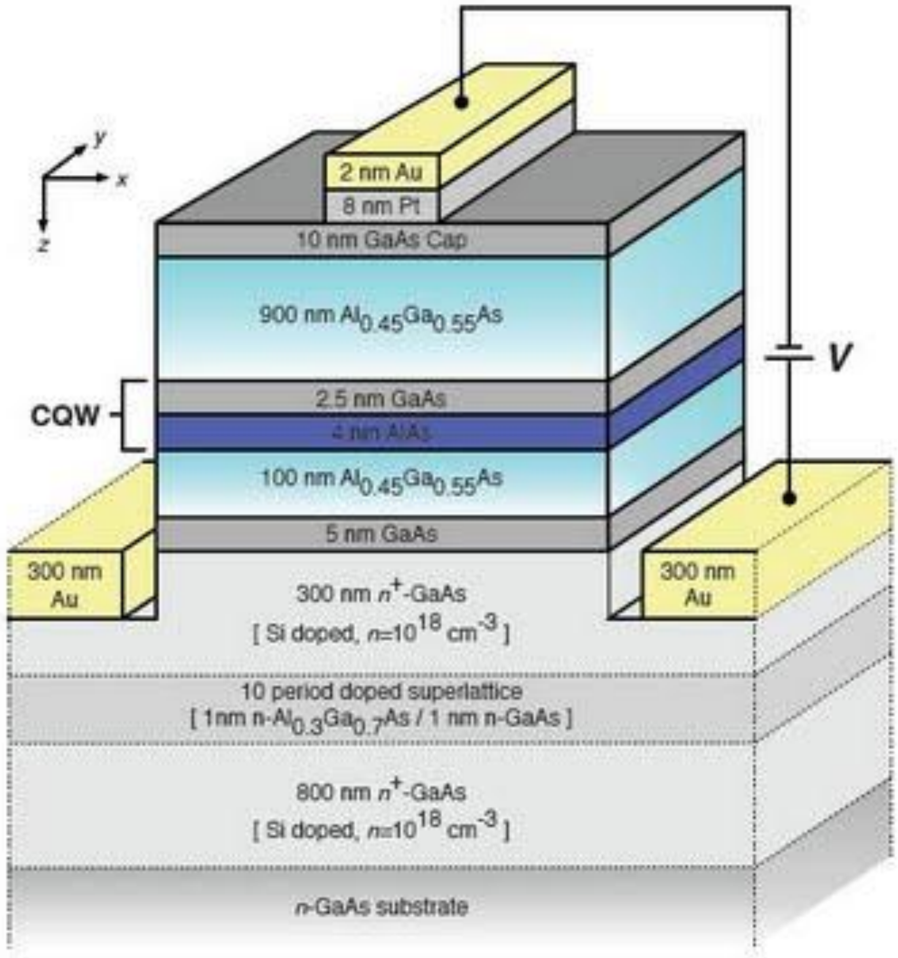
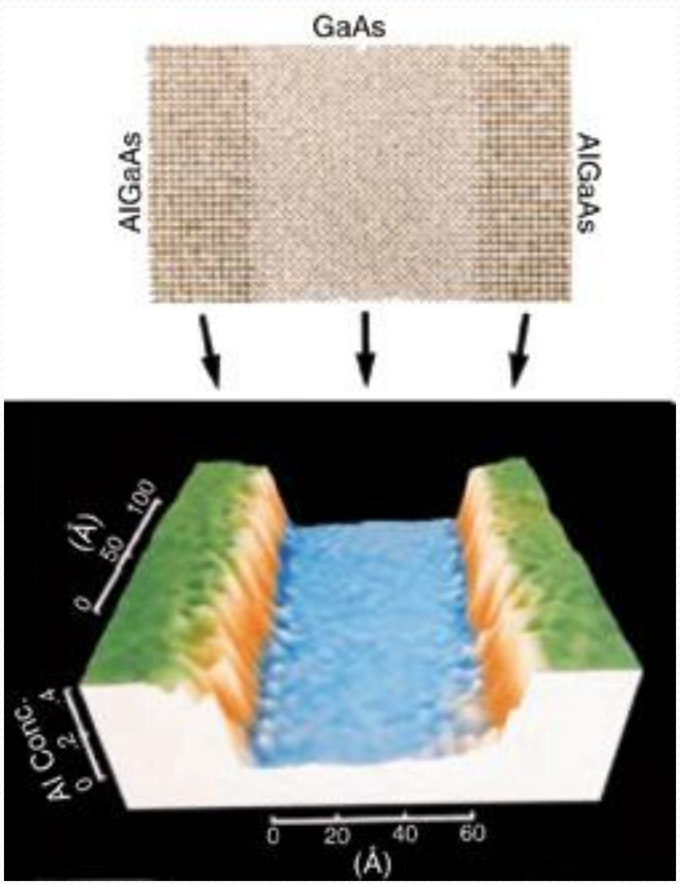
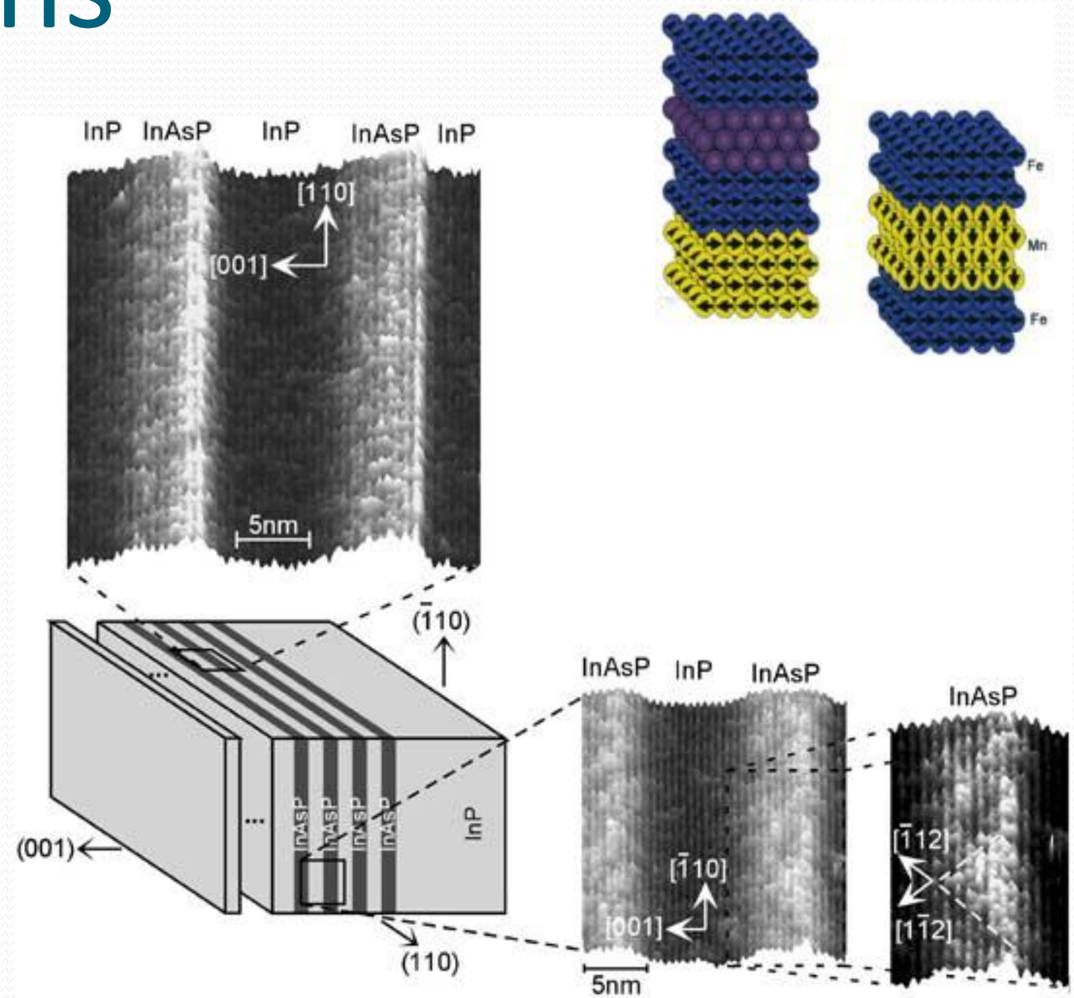
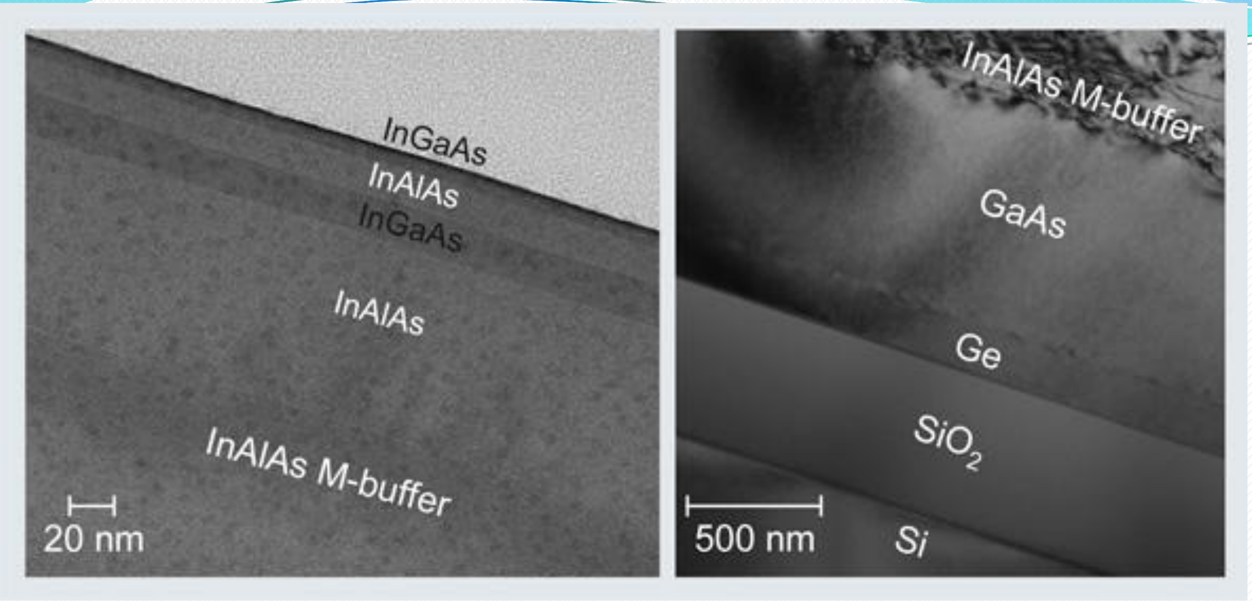


FIG. 1: The layer structure of the coupled quantum well device.

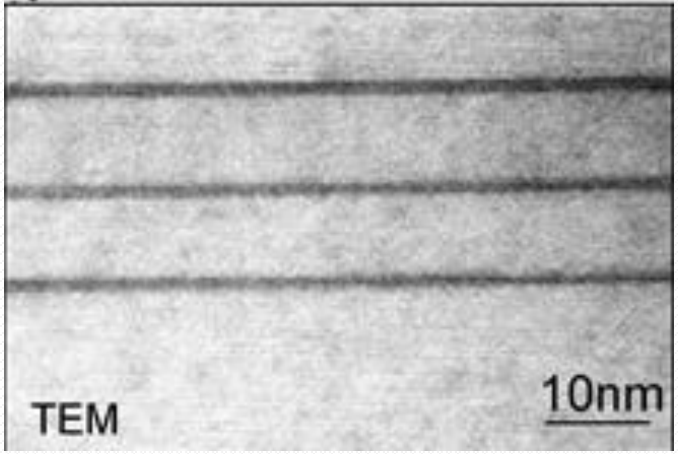
Heterojunctions

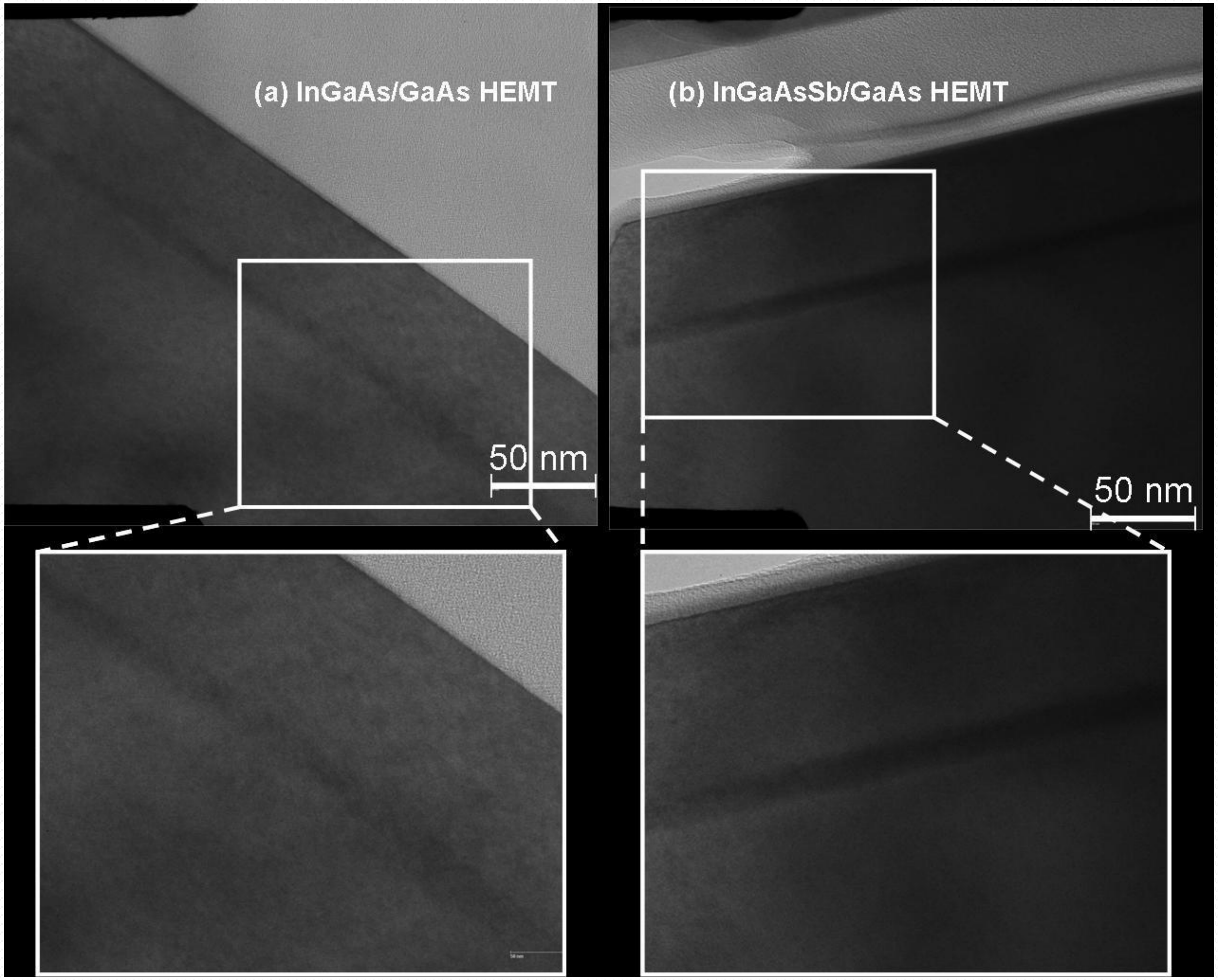


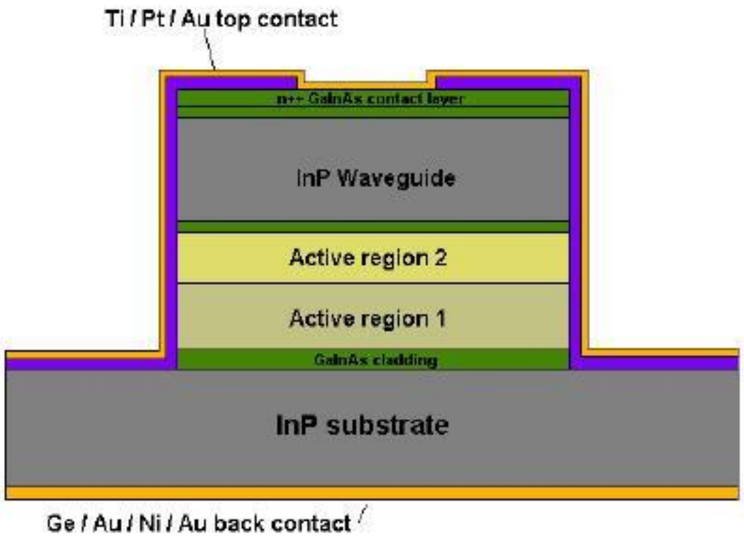


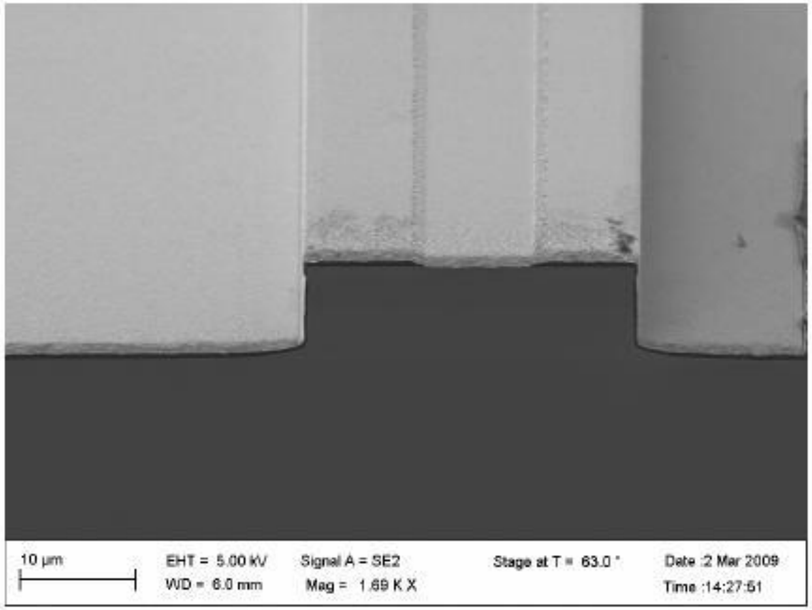


quantum well structure




(a) InGaAs/GaAs HEMT
50 nm
(b) InGaAsSb/GaAs HEMT
50 nm


Ti / Pt / Au top contact
n++ GaInAs contact layer
InP Waveguide
Active region 2
Active region 1
GaInAs cladding
InP substrate
Ge / Au / Ni / Au back contact


10 µm
EHT = 5.00 kV
WD = 6.0 mm
Signal A = SE2
Mag = 1.69 K X
Stage at T = 63.0 °
Date :2 Mar 2009
Time :14:27:51

Key Concept: Band diagram

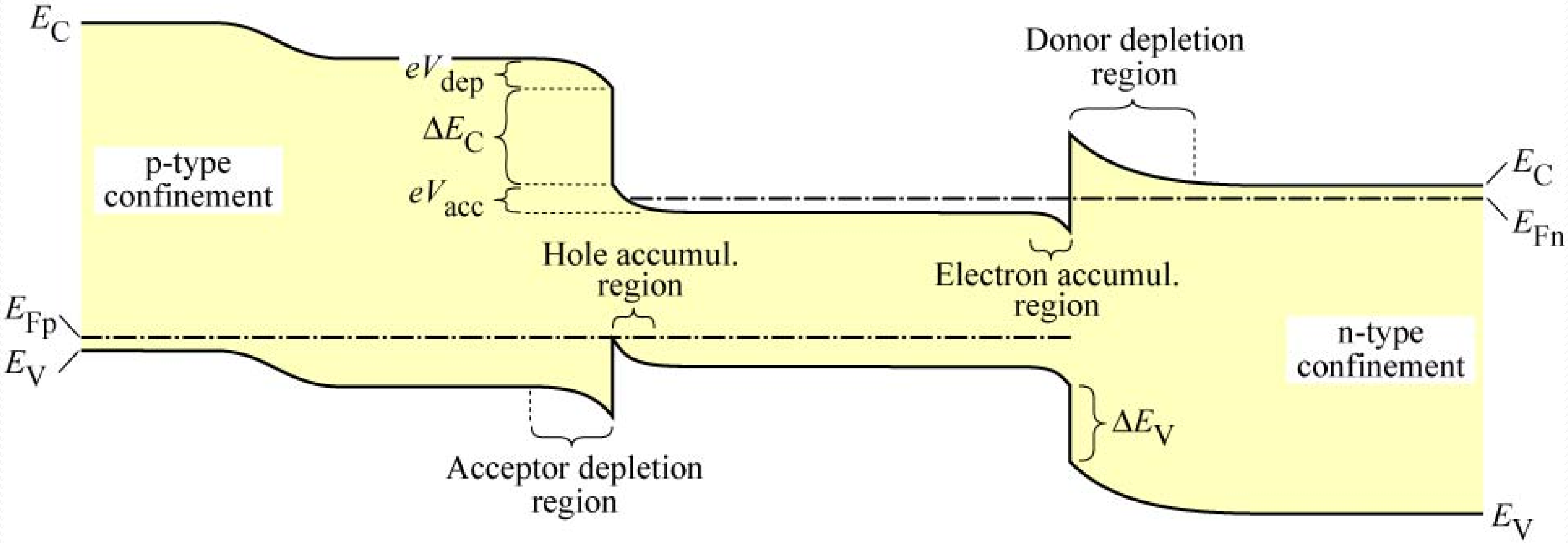
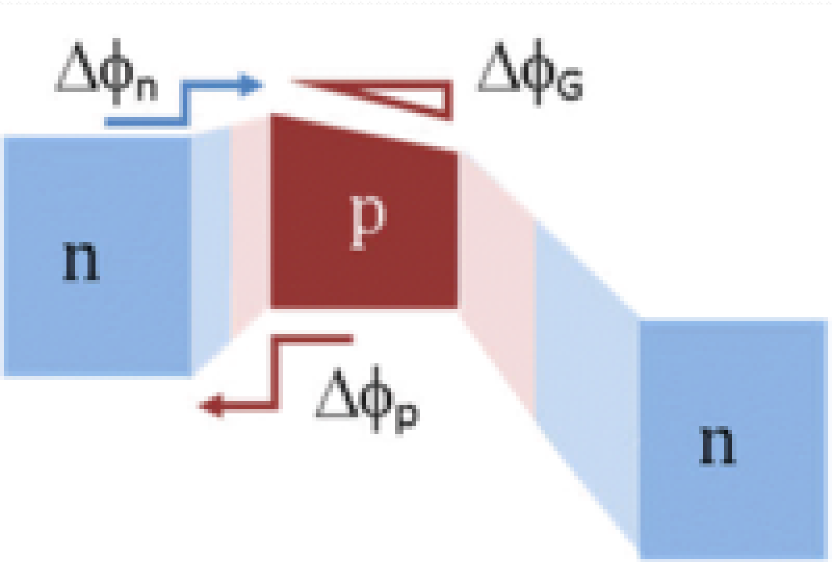
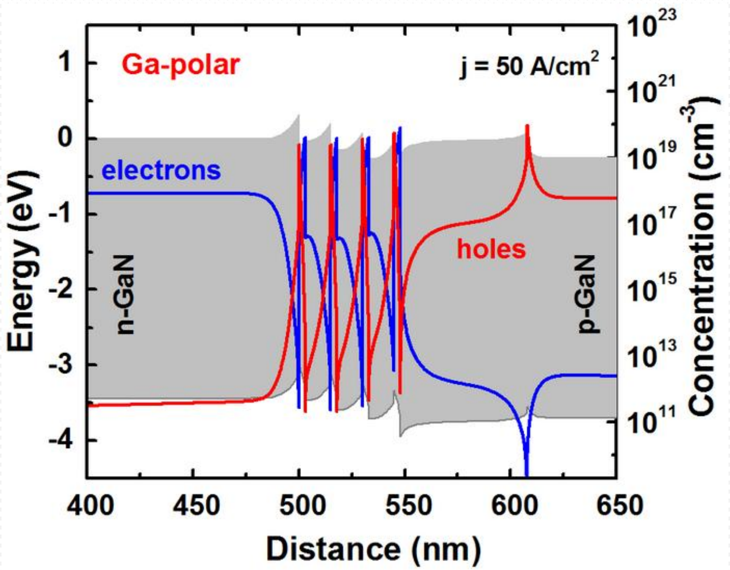


Fig. 7.9. Band diagram of a forward-biased double heterostructure. The p-type confinement layer consists of a lightly doped layer close to the active region and a higher doped layer further away from the active layer (adapted from Kazarinov and Pinto, 1994).

- Conduction band, valence band, and sometimes other band (S-O)
- Electron and hole distribution

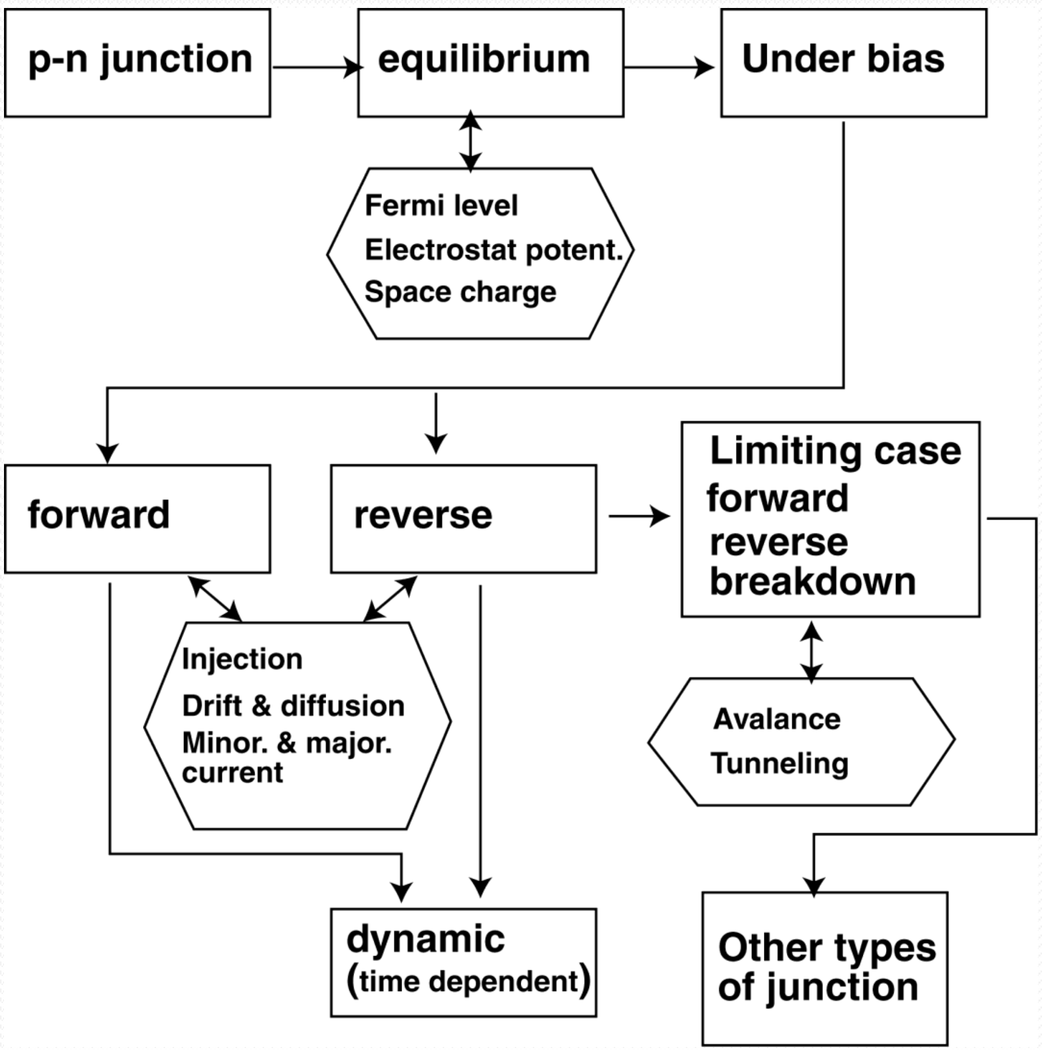




How to plot band diagram

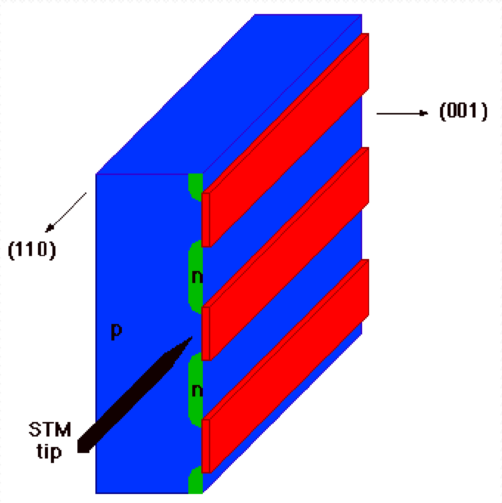
- Calculate conduction band and valence band
- Determine Fermi levels in each layer
- Calculate electrostatic potential and depletion width (if relevant) at each junction interface
- Apply principle of detailed balancing: line up the Fermi level (for device at thermal equilibrium or at rest - inactive)
- Calculate the carrier density profile
- Apply the steps for active device with injected excess carriers and/or bias

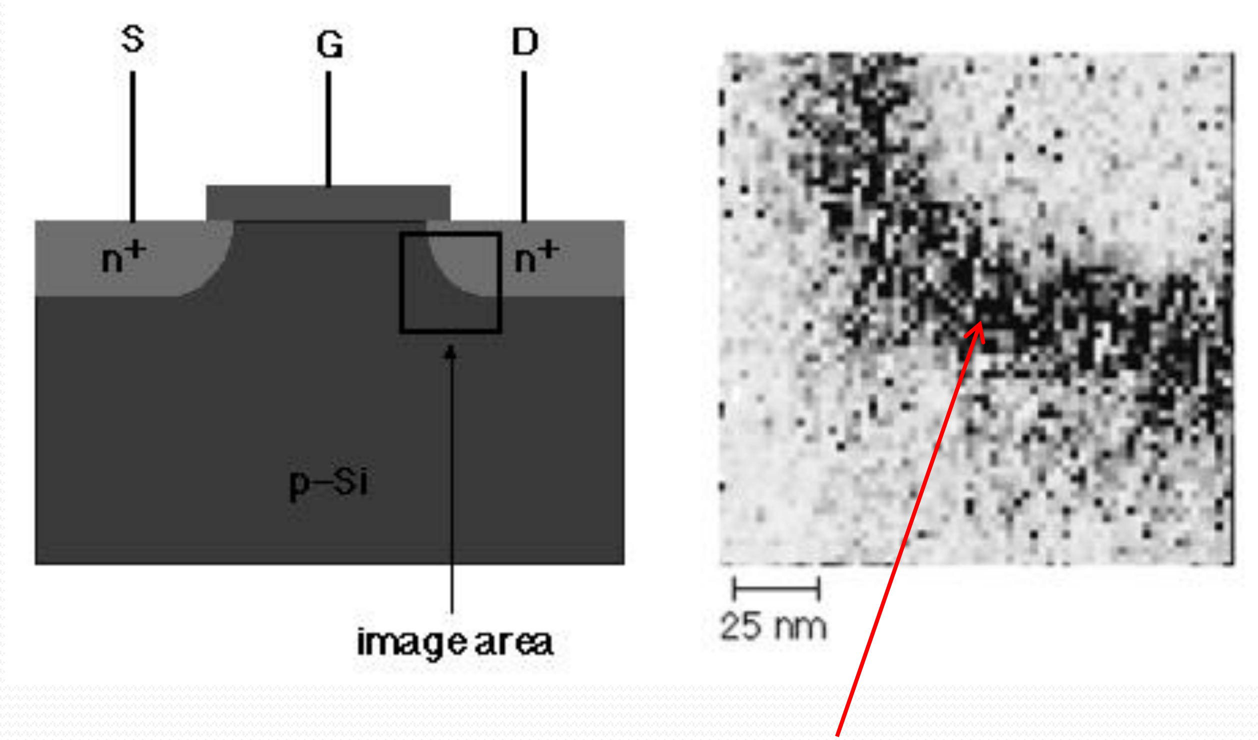
Study topics in p-n junction



p-n Junction

Scanning Tunneling Microscope image of a junction





Existence of the depletion layer

Current at equilibrium

$$\Rightarrow \quad J_n(x) = e\mu_n n(x)E(x) + eD_n \frac{dn}{dx} = 0$$

Drift Diffusion

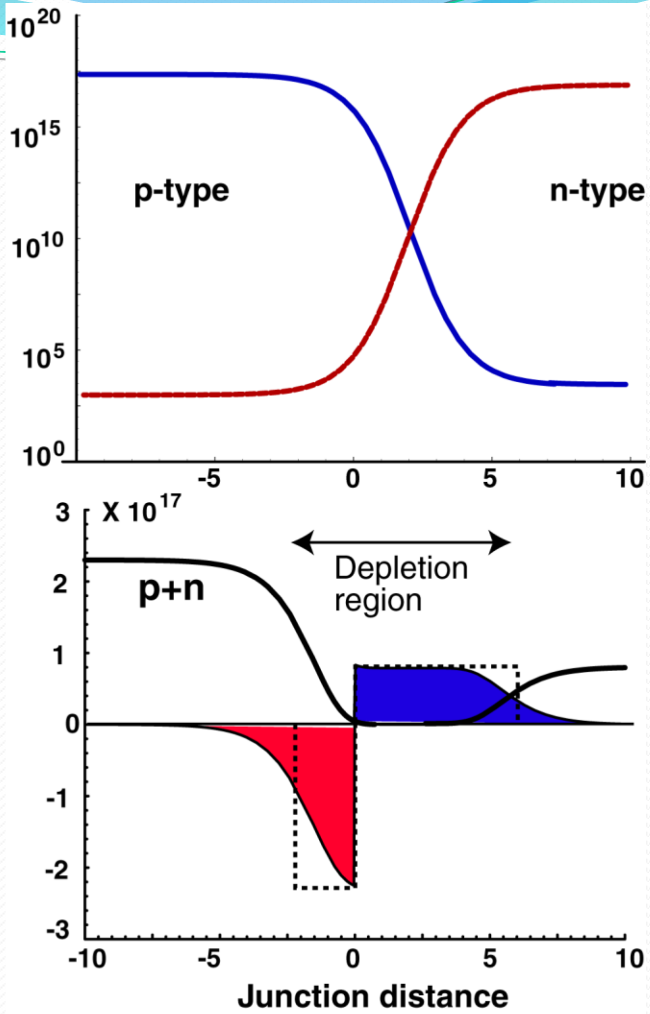
Solving for n(x) vs. E field

$$\frac{d \ln n(x)}{dx} = -\frac{e}{k_B T} E(x) = \frac{e}{k_B T} \frac{dV(x)}{dx}$$

Electrostatic potential

$$\ln n(x) = \frac{e}{k_B T}\left[V(x) + v\right]$$

$$\Rightarrow \quad n(x) = n_{-\infty} e^{eV(x)/k_B T}$$



We have exactly the same equation for p

$$p(x) = p_{-\infty} e^{-eV(x)/k_B T}$$

Important carrier relation:

$$n(x)p(x) = n_{-\infty}p_{-\infty} = n_n p_n = n_p p_p$$

$$\Rightarrow \ln n(x) + \ln p(x) = \text{constant}$$

Approximation for the depletion region

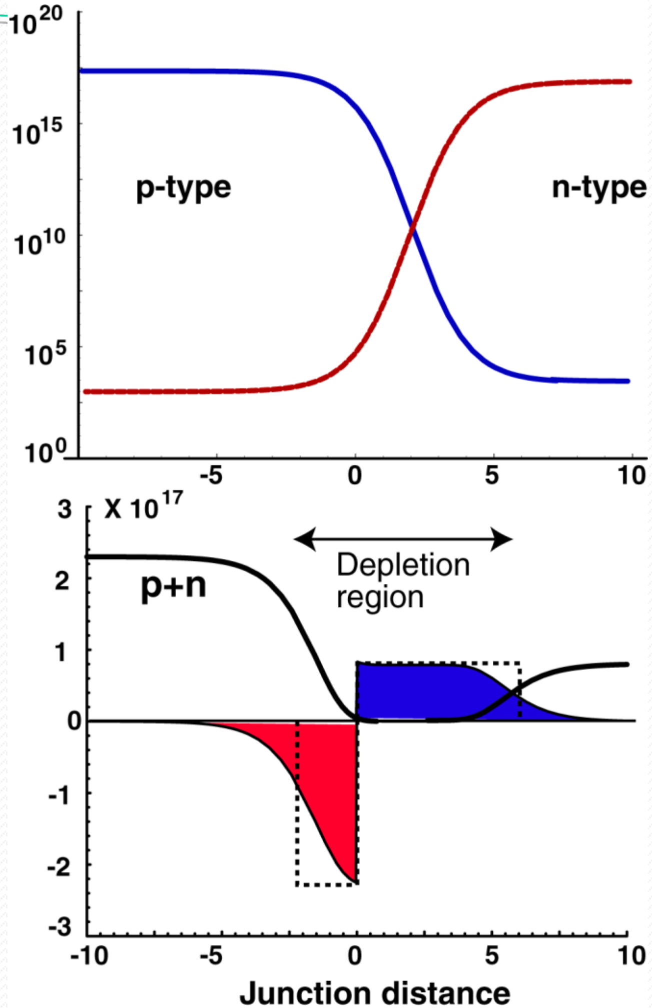
The electrostatic Poisson equation

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon} = -\frac{e}{\varepsilon}\left[N_D(x) - N_A(x)\right]$$

Uniform doping

$$\phi(x) = \frac{eN_A}{2\varepsilon}\left(x + x_p\right)^2 \qquad x \in \left[-x_p \quad 0\right]$$

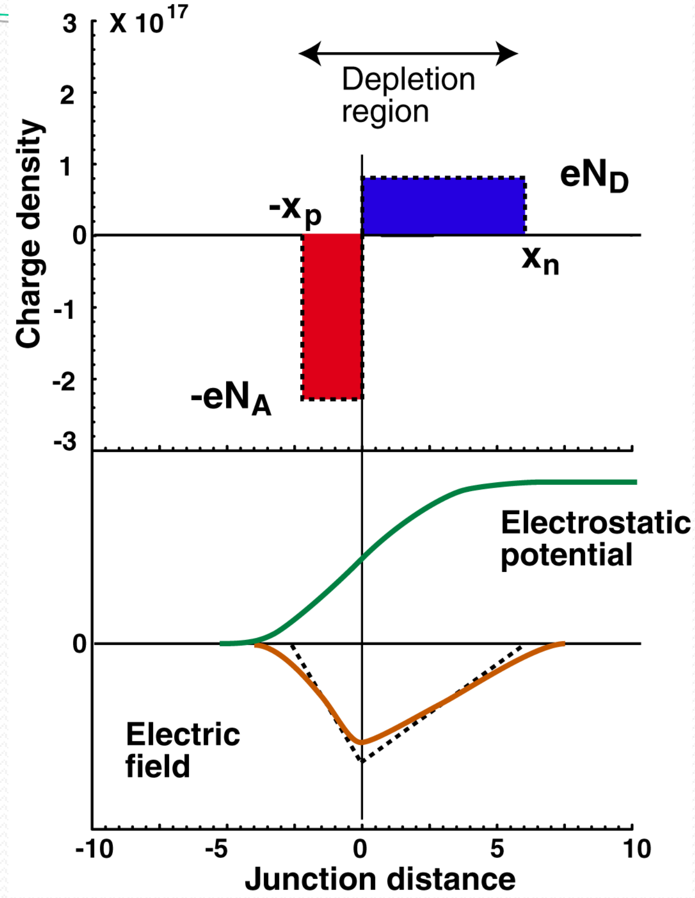
$$\phi(x) = V_o - \frac{eN_D}{2\varepsilon}\left(x - x_n\right)^2 \qquad x \in \left[0 \quad x_n\right]$$



$$\phi(0) = V_o - \frac{eN_D}{2\varepsilon} x_n^2 = \frac{eN_A}{2\varepsilon} x_p^2$$

Then $$V_o = \frac{eN_D}{2\varepsilon} x_n^2 + \frac{eN_A}{2\varepsilon} x_p^2$$

The charge sheet density is $$|Q| = eN_A x_p = eN_D x_n$$



Solving the equation for xn and xp

$$x_p = \frac{N_D}{N_D + N_A} W \quad ; \quad x_n = \frac{N_A}{N_D + N_A} W$$

Depletion width $$x_p + x_n = W = \sqrt{\frac{2\varepsilon V_o}{e}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}$$

$$x_p + x_n = W = \sqrt{\frac{2\varepsilon a_B e V_o}{e^2}\left(\frac{1}{a_B N_D} + \frac{1}{a_B N_A}\right)}$$

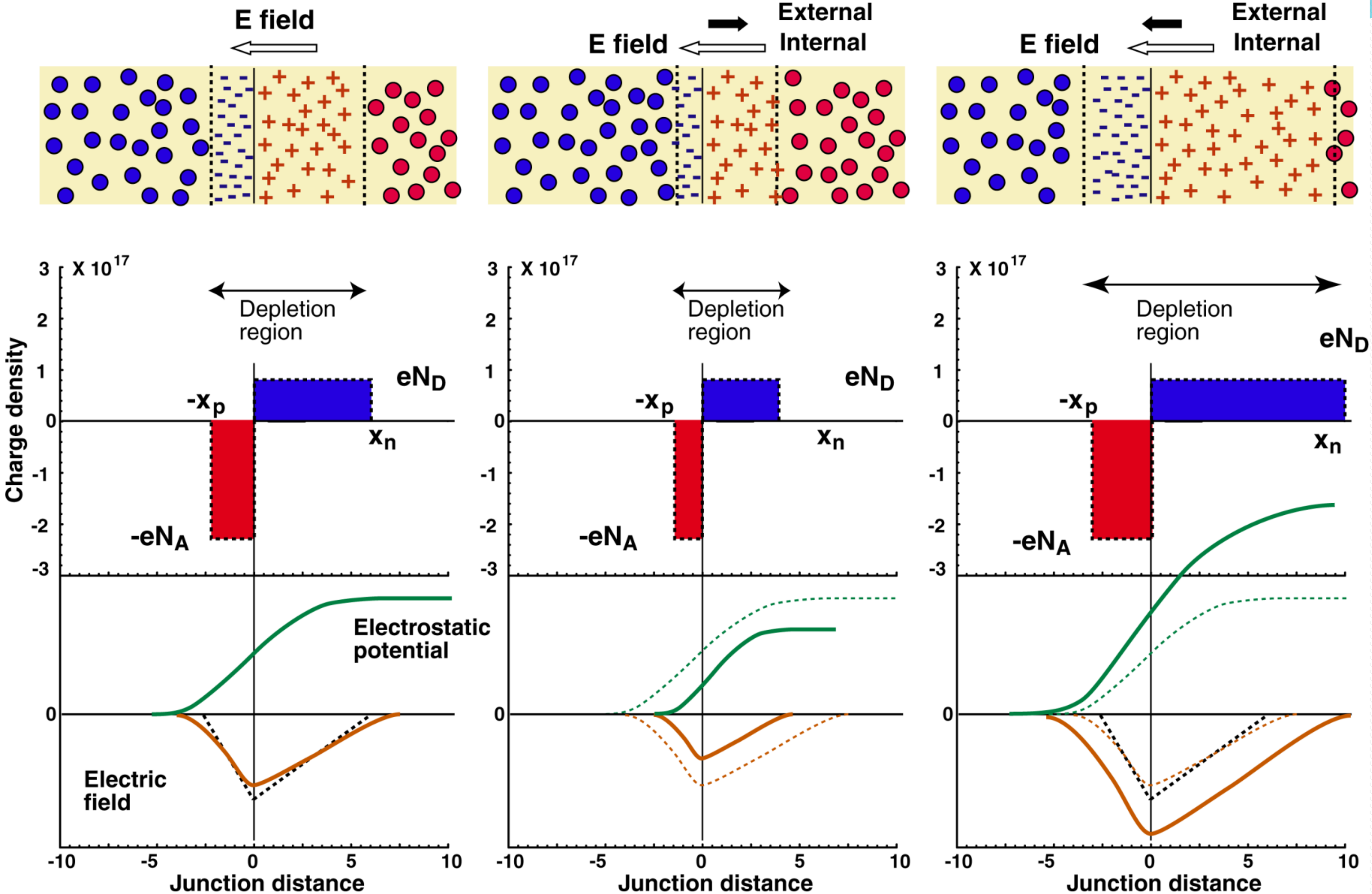
$$x_p + x_n = W = \sqrt{\frac{eV_o}{(R_\infty / \varepsilon)}}\sqrt{\left(\frac{1}{a_B N_D} + \frac{1}{a_B N_A}\right)}$$

Summary of key features

- At junctions: electron diffuses to p-side and hole diffuse to n-side. They recombine (cancel each other out) in the middle, resulting in a carrier depletion region
- Without carriers in the depletion region, space charge from ionized donors and acceptors appears, resulting in electrostatic field and potential. Net charge is still and always zero.
- The larger the depletion width, the more space charge exposed, the higher the electrostatic field and potential.
- Vice versa, the carriers continue to diffuse and enlarge the depletion width until the build up electrostatic field and potential are strong enough to counter the carrier diffusion pressure: equilibrium is reached
- Carrier diffusion "potential" is negatively proportional to the depletion width. The electrostatic potential is ~ x^2. Therefore, the depletion width is ~ square root of electrostatic potential. Similarly, higher dopant density → higher electrostatic potential → smaller depletion width.
- External bias reducing the internal field: smaller depletion width, higher diffusion current; Ext. bias enhances the internal field: larger depletion width, lower diffusion

Junction – Part 1

Lecture 2

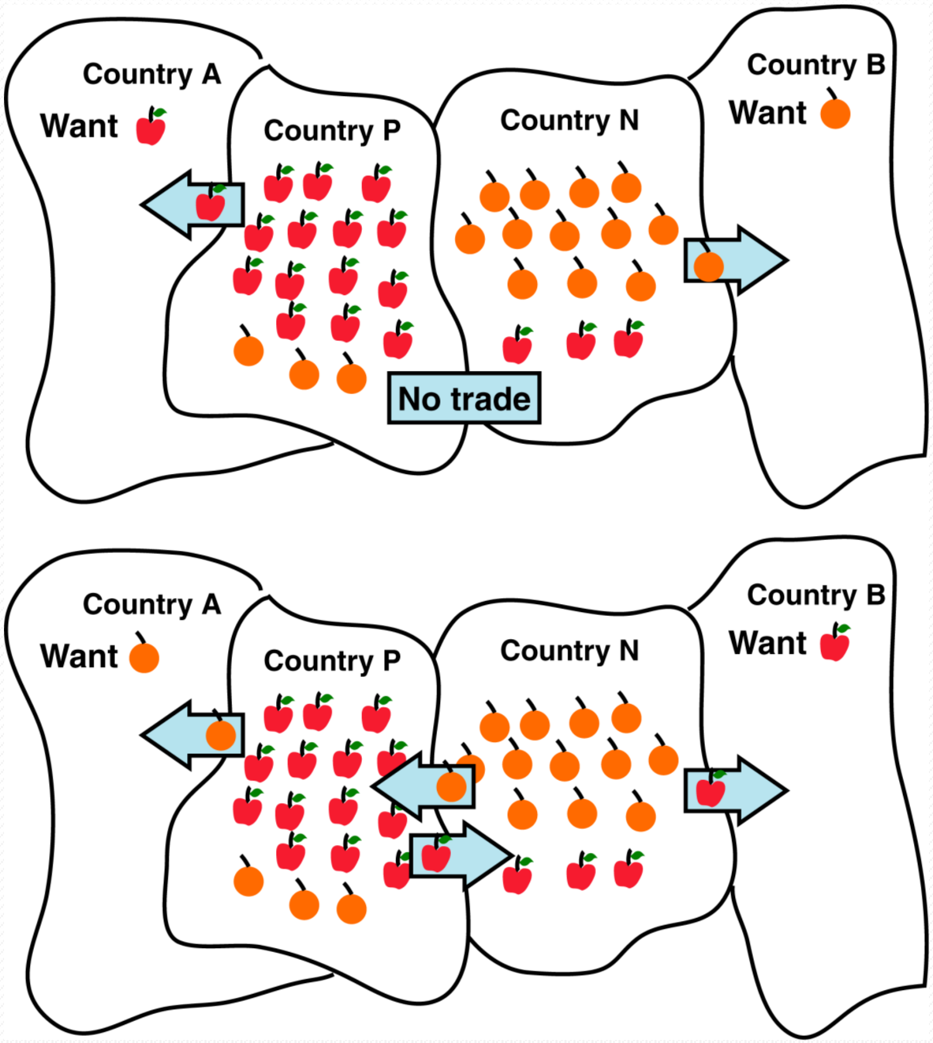


Equilibrium

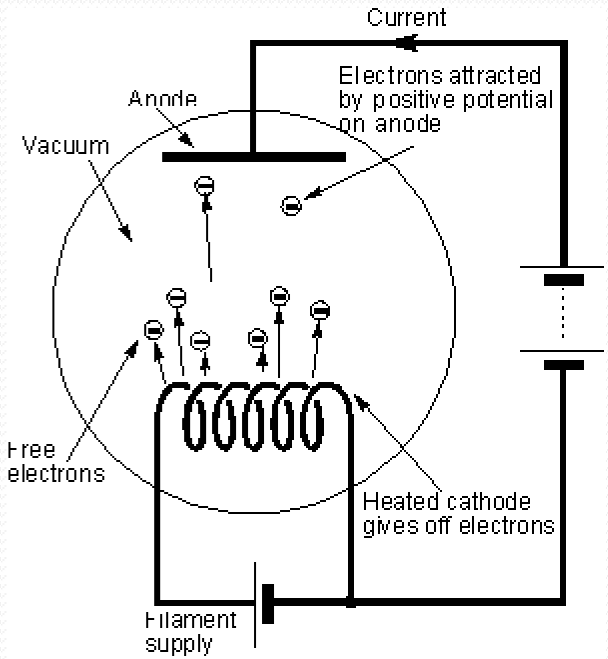
Forward bias: non-equilibrium current ≠ 0

Reverse bias non-equilibrium current flow ≠ 0

A non-technical analogy



The vacuum tube diode



Only the cathode side with the hot filament can emit electrons for current flow.
The anode cannot emit electron

A similar principle for semiconductor p-n junction diode

Let's look at the figure→. Why is there light at the junction? That's where electrons and holes recombine and give off photons. Why is there light in the n⁻ and n⁺ region? There must be holes there as well (for sure there are electrons there). Holes indeed travel quite a bit, don't they? The vertical scale is logarithmic, so the linear slope indicates approximately spatial exponential profile. Recalling Chapter IV, that 1-D carrier diffusion in steady state is described as $p(x) = p_1 e^{-x/L_D} + p_o$.

<u>So it looks like diffusion! Diode current includes hole diffusion current (minority carrier) in an n-region (electron is the majority carrier).</u> At 100 A/cm², assuming steady state, the slope in the n⁻ region indicates a diffusion length of? Let's see:

$\Delta x = 80\ \mu m$; $\Delta \log_{10}(y) = 1$; So $\Delta \ln(y) / \ln(10) = 1$; or

$\Delta \ln(y) = \ln(10) = 2.3$; since $y = e^{-x/L}$; $\ln y = -x/L$;

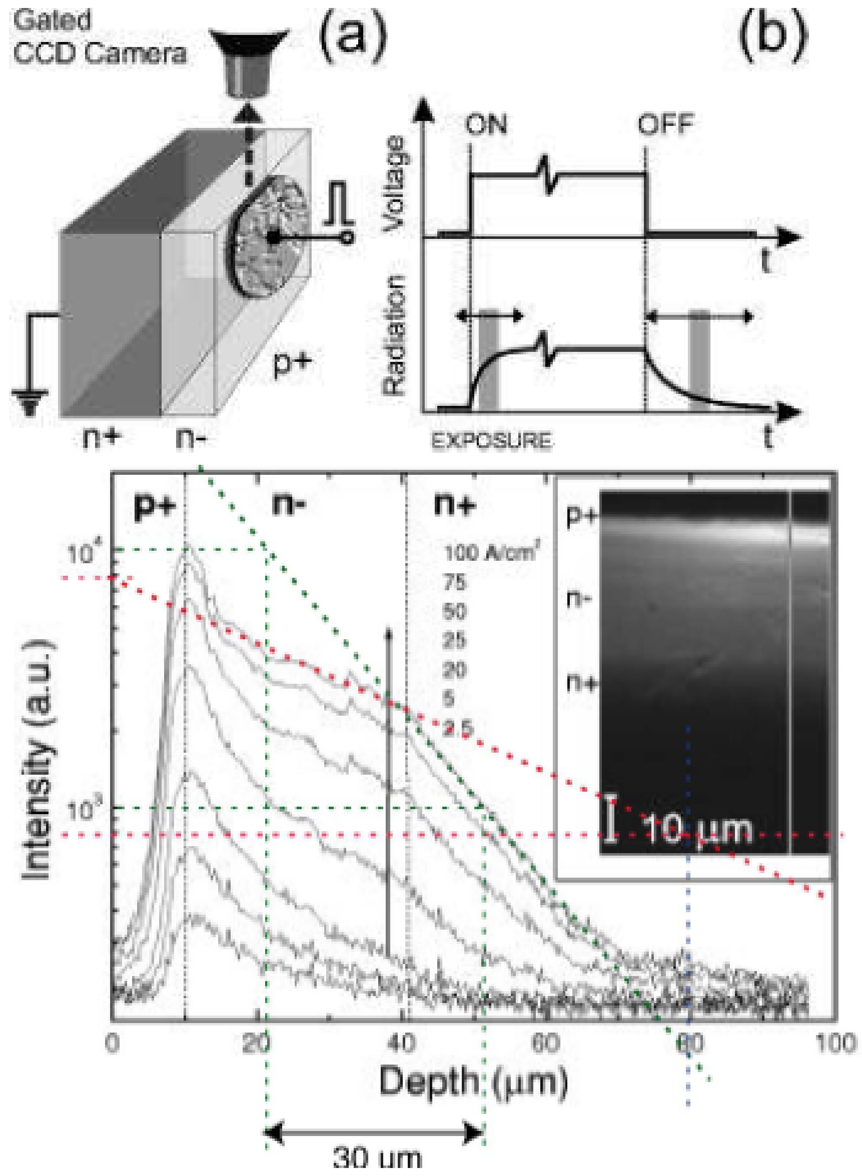
$L_{n^-} = \dfrac{\Delta x}{\Delta \ln y} = \dfrac{80\ \mu m}{2.3} \approx 35\ \mu m$. Similarly:

$L_{n^+} = \dfrac{30\ \mu m}{2.3} \approx 13\ \mu m$. The researchers reported 15 um.

Close enough!

Key points: It looks like that holes diffuse from p+ across the junction into the n-regions, and this is the forward bias current. So, to find out the diode current under forward bias<u>, we must determine the diffusion current.</u>

This will be what we do NEXT→



Excess carrier distribution (chapter 4, and above):

$$p_{ne}(x) = p_{ne}(x_n)e^{-(x-x_n)/L_p}$$

At x_n, $p_n(x_n) \approx N_V e^{-(E_{F1}-E_{V2})/k_BT}$ **. At equilibrium:**

$p_{no}(x_n) \approx N_V e^{-(E_{F2}-E_{V2})/k_BT}$ **. The excess carrier is:**

$$p_{ne}(x_n) = p_n(x_n) - p_{no}(x_n) = p_{no}(x_n)\left[e^{(E_{F2}-E_{F1})/k_BT} - 1\right]$$

$$p_{ne}(x_n) = p_{no}(x_n)\left[e^{eV_b/k_BT} - 1\right]$$

$$p_{ne}(x) = p_{no}(x_n)\left[e^{eV_b/k_BT} - 1\right]e^{-(x-x_n)/L_p}$$

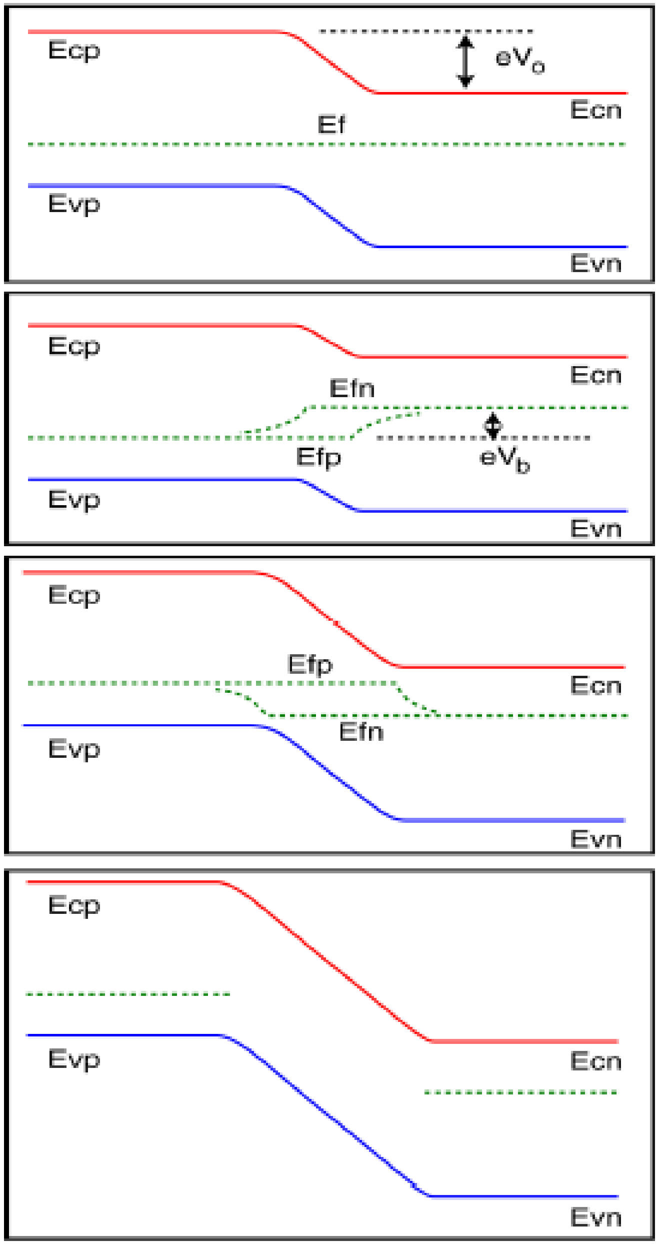
Diffusion current:

$$J_{pe} = -eD_p \frac{dp_{ne}(x)}{dx} = e\frac{D_p}{L_p} p_{no}(x_n)\left[e^{eV_b/k_BT} - 1\right]e^{-(x-x_n)/L_p}$$

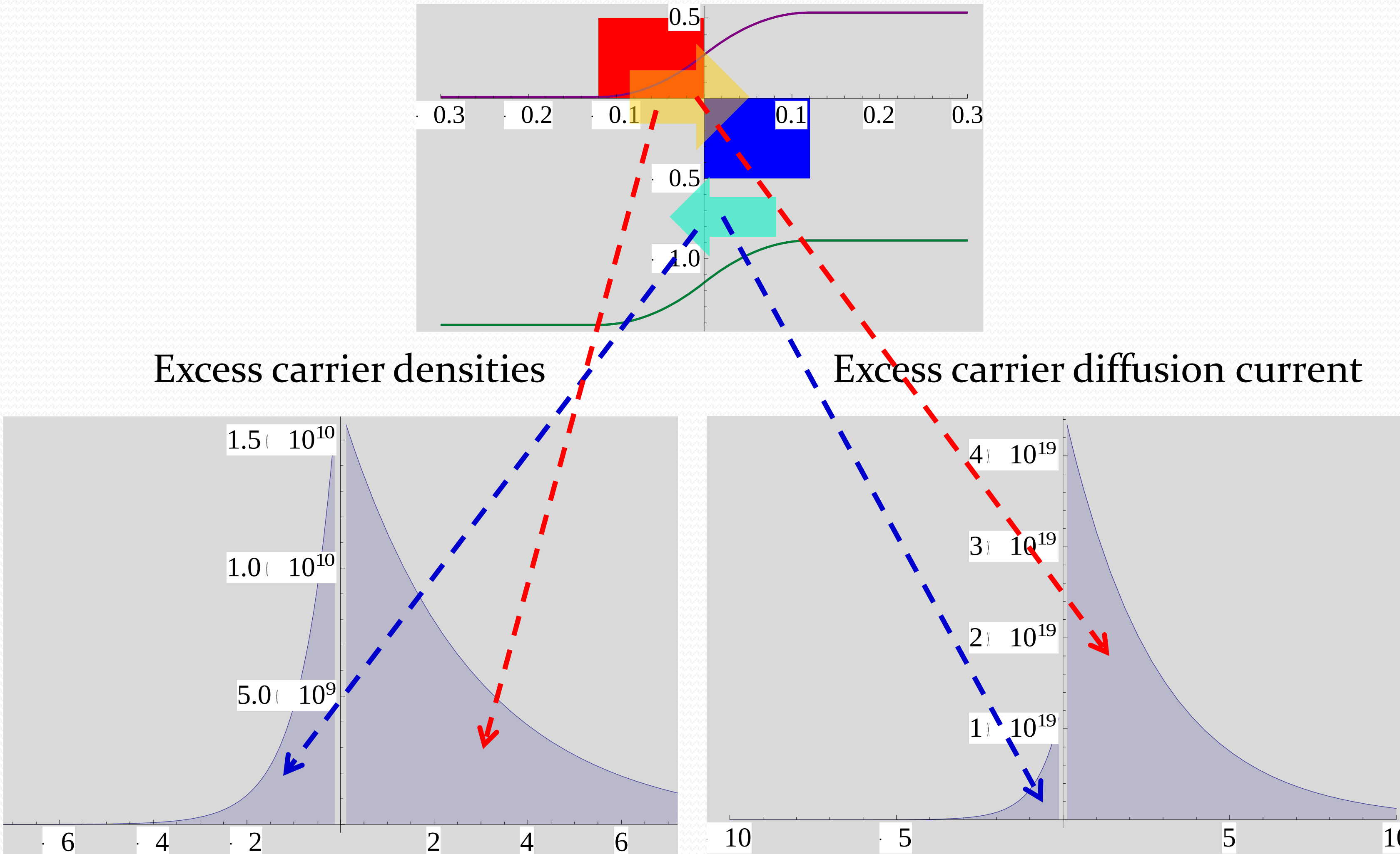
$$J_{pe}\Big|_{x_n} = e\frac{D_p}{L_p} p_{no}(x_n)\left[e^{eV_b/k_BT} - 1\right].$$

Similarly for electron current:

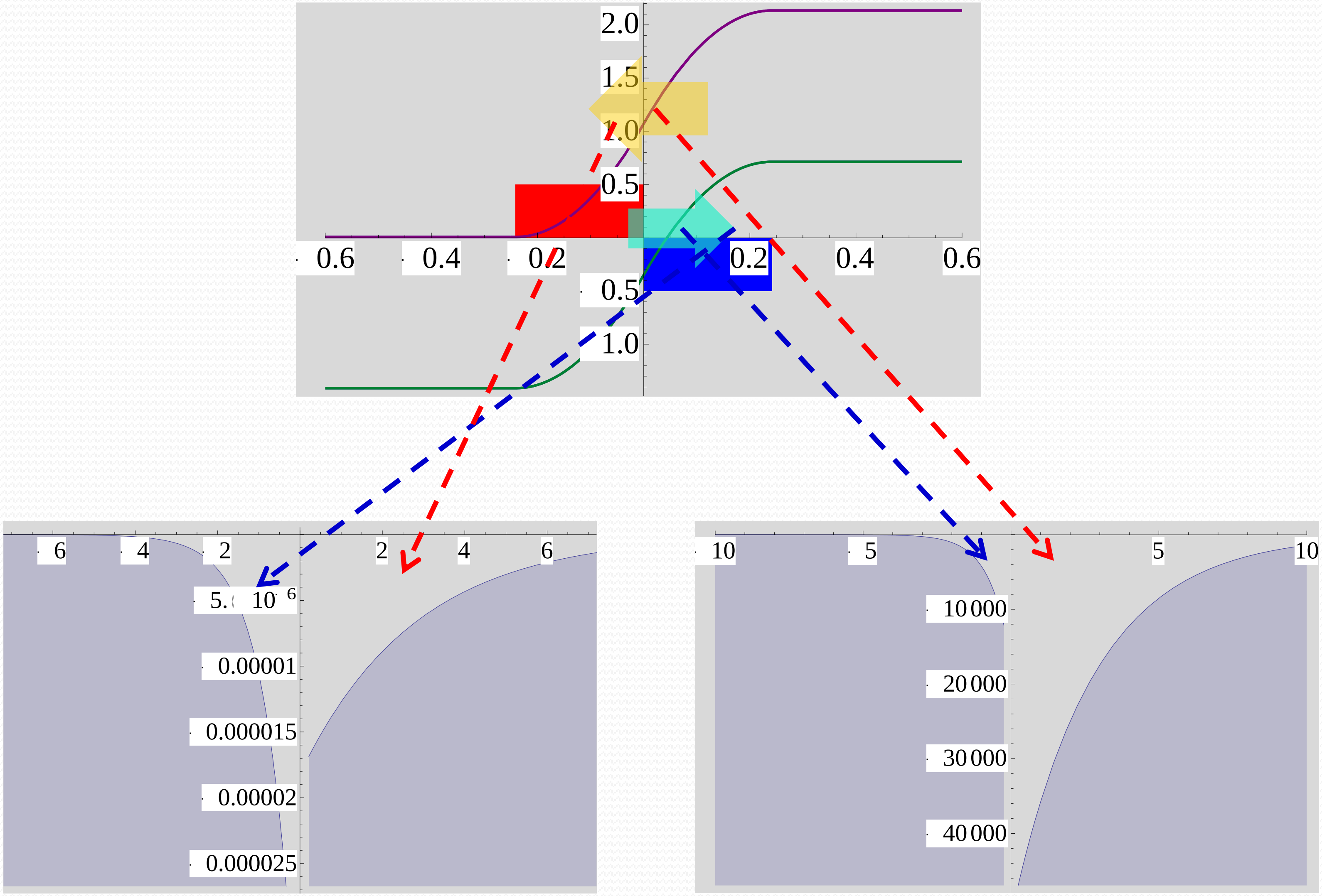
$$J_{ne}\Big|_{x_n} = -e\frac{D_n}{L_n} n_{po}(-x_p)\left[e^{eV_b/k_BT} - 1\right]$$



Diffusion current density



Current for reverse bias



$$J_{ne} = eD_p \frac{dn_{pe}(x)}{dx} = e\frac{D_n}{L_n} n_{po}(-x_p)\left[e^{eV_b/k_BT} - 1\right] e^{(x+x_p)/L_n}$$

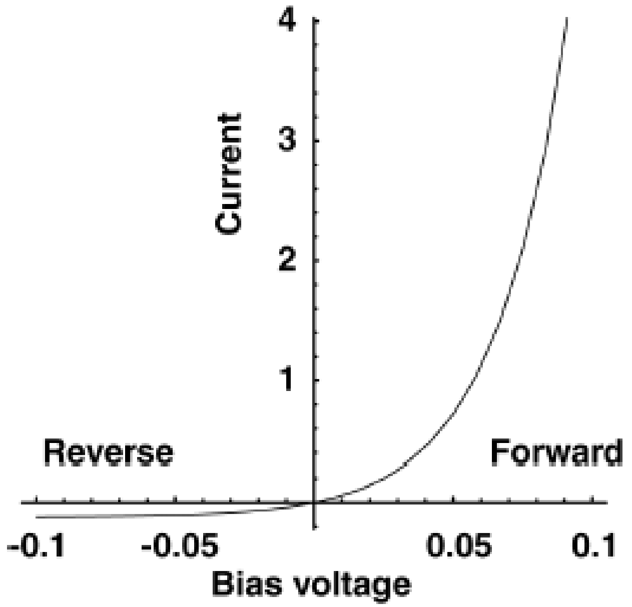
$$J_{ne}\big|_{-x_p} = e\frac{D_n}{L_n} n_{po}(-x_p)\left[e^{eV_b/k_BT} - 1\right]$$

Total diode current $= J_{ne}\big|_{-x_p} + J_{pe}\big|_{x_n} =$

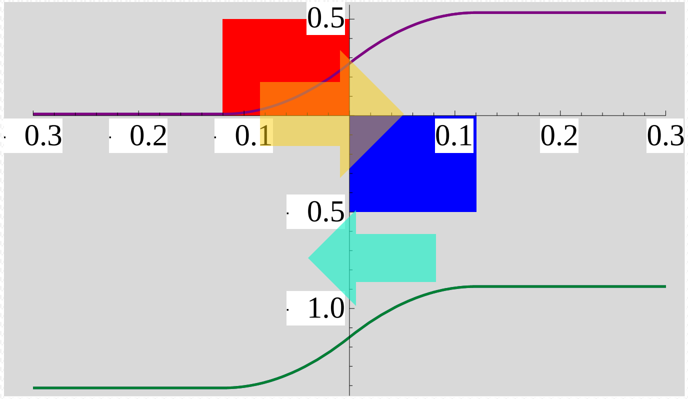
$$J = e\left(\frac{D_n}{L_n} n_{po} + \frac{D_p}{L_p} p_{no}\right)\left[e^{eV_b/k_BT} - 1\right]$$

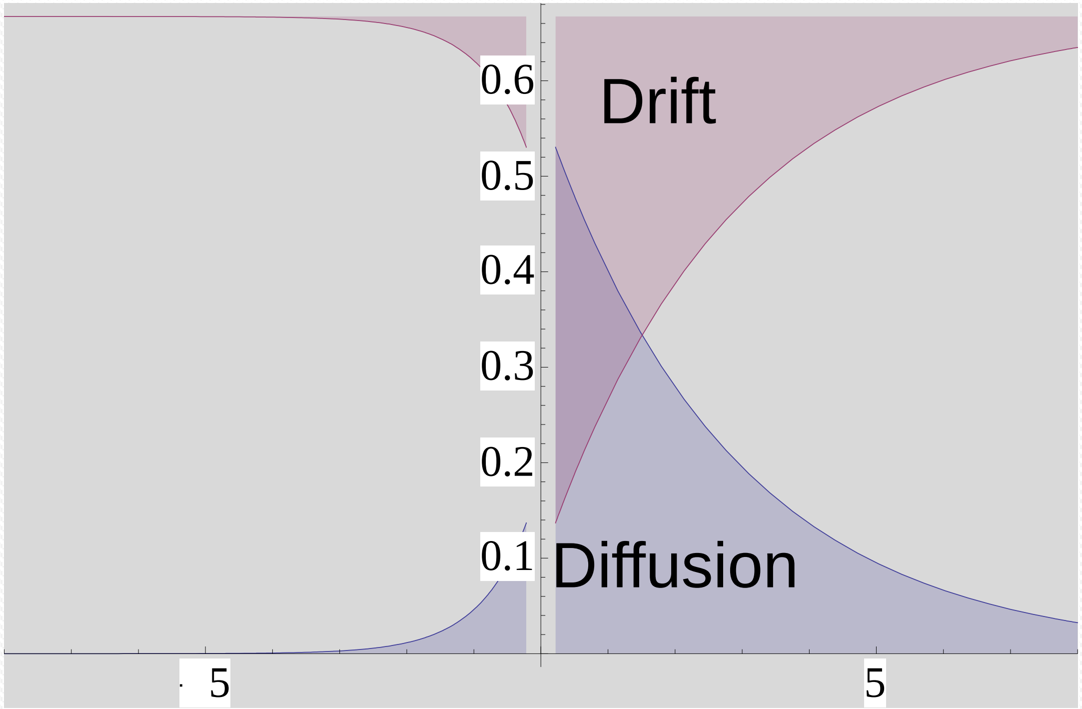
$$J \cong e n_i^2\left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)\left[e^{eV_b/k_BT} - 1\right]$$

This is the ideal diode equation. This eq. is valid for the any polarity, i. e. reverse bias also.



Drift and diffusion current





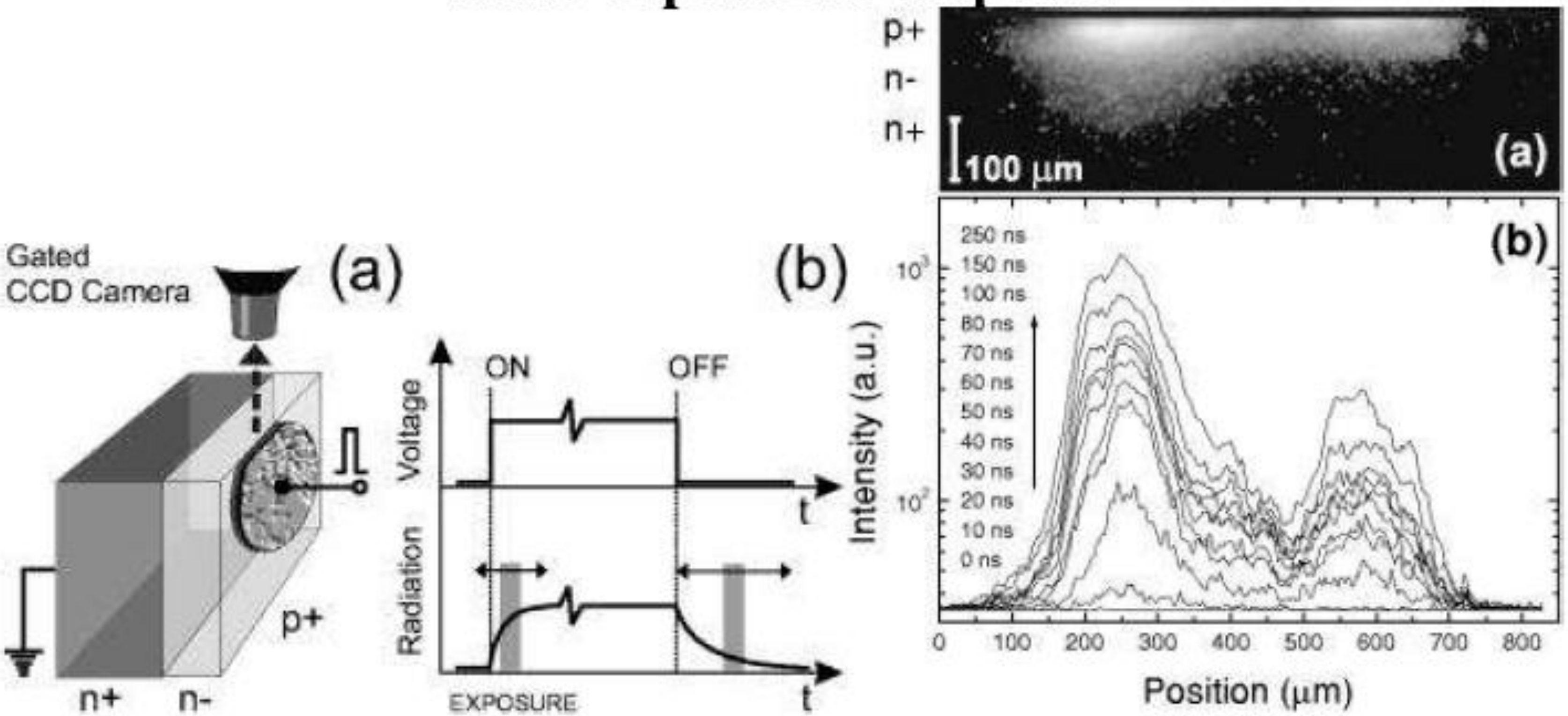
Ideal diode key features

- An external electric field will disturb the equilibrium at junctions. Carriers want to return to equilibrium. Continuous injection (pumping) of carrier is necessary to maintain non-equilibrium condition: current flows to maintain a steady state
- Excess holes must diffuse to n-side and excess electrons must diffuse to p-side. Diffusion current is much larger than drift current across the junction. In one dimension, the diffusion profile is ~ exponential vs. distance.
- Hole current in n-region and electron current in p-region are called minority carrier currents.

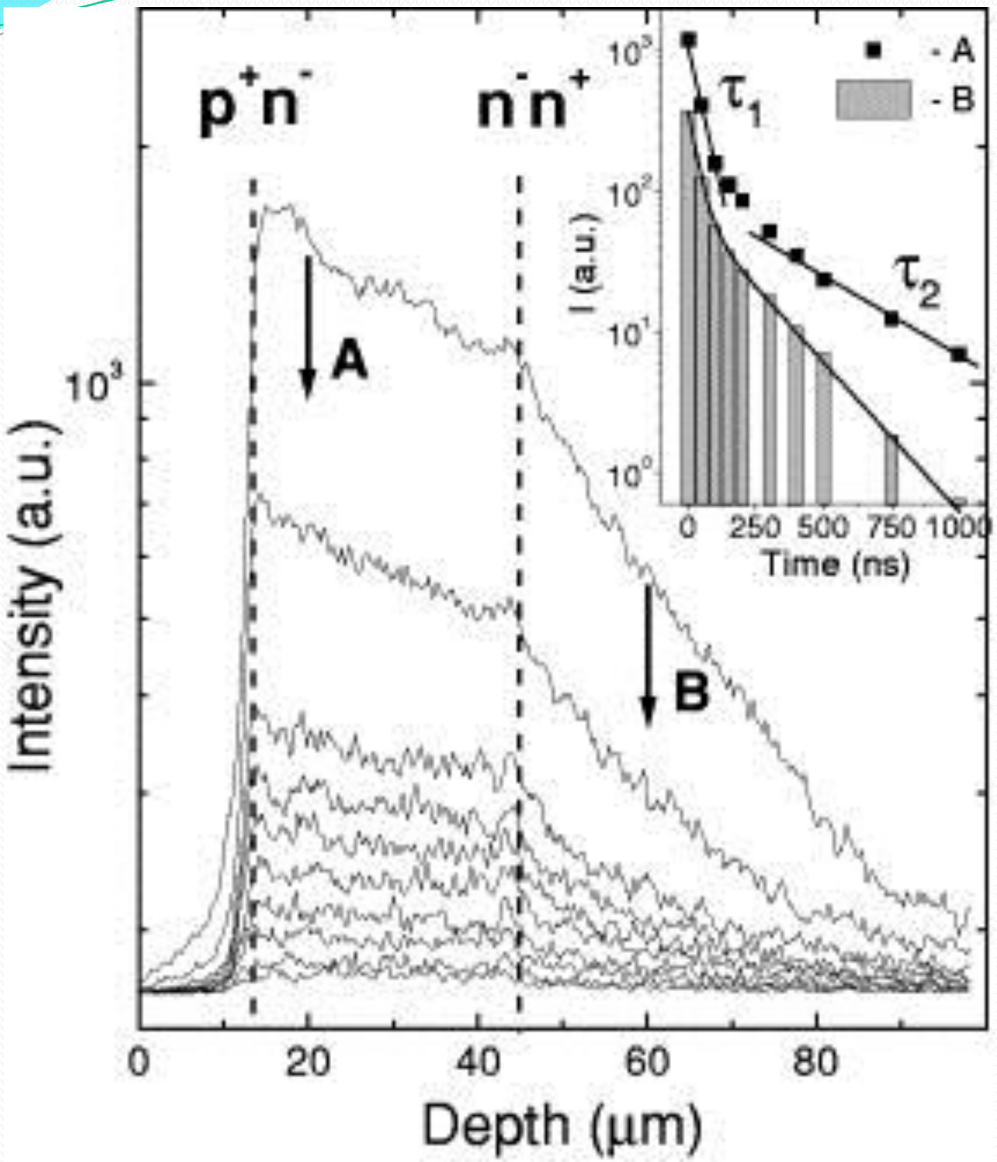
Ideal diode key features (continued)

- The diffusion current is proportional to the excess carrier density. The excess carrier density is approximately exponentially dependent on the difference between quasi-Fermi levels which is the bias voltage. Therefore, forward bias current is exponentially dependent on bias voltage.
- On reverse bias, there is no excess current (*may be we should call deficiency current!*). Holes from n-region and electrons from p-region (minority carriers) carry the current: very small and quickly saturate.
- On forward bias, weaker internal electric field the depletion width is reduced as the junction potential drop is reduced. On reverse bias, the depletion width increases with larger potential drop

Time-dependent response



The figures show clearly that diode current cannot be turned on or off instantaneously. It takes time for the carriers to charge, build up, and discharge and decay.



- Time behavior, space-time carrier distribution. (note slope change). Time dependent diffusion.
- Exponential behavior vs. both space and time. This is a combination of diffusion, decaying, and discharge.

Time dependent response

Mechanisms:

- Capacitive effects (charge and discharge)
- Carrier lifetime effects

Description

P: Pump rate
τ is the carrier lifetime

Diffusion

Continuity equation:

$$\frac{\partial n}{\partial t} = P - \frac{n}{\tau} + D\nabla^2 n = P - \frac{n}{\tau} - \nabla \bullet \mathbf{F}$$

no external pumping, current continuity: (n or p with charge sign change) $\nabla \bullet \mathbf{J}_{(\mathrm{n\ or\ p})} = e\frac{\partial n}{\partial t} + e\frac{n}{\tau}$

For one-D approx.: $\frac{\partial J}{\partial x} = e\frac{\partial n}{\partial t} + e\frac{n}{\tau}$ or $\frac{\partial I}{\partial x} = Ae\frac{\partial n}{\partial t} + Ae\frac{n}{\tau}$

Time dependent response (cont.)

Integration:

$$I(x,t) = Ae\frac{\partial}{\partial t}\int^{x} n(\xi,t)\,d\xi + Ae\frac{1}{\tau}\int^{x} n(\xi,t)\,d\xi$$

Since:

$$\int^{x} n(\xi,t)\,d\xi \equiv Q(x,t)$$

Space dependent charge

Time dependent response (cont.)

$$I(x,t) = \frac{\partial Q(x,t)}{\partial t} + \frac{Q(x,t)}{\tau}$$

Capacitive effect: Charge time-dependent term due to migration, drift or diffusion:

Charge lifetime (decaying term)

At x-> infinity

$$I_{net}(t) = \frac{\partial Q(t)}{\partial t} + \frac{Q(t)}{\tau}$$

Time dependent response (cont.)

Solving the diff Eq. $$Q(t) = \int^{t} dt' \, I(t') e^{(t'-t)/\tau}$$

This term signifies the net charge decayed due to lifetime; finite time response.
For circuit response: need to know capacitance. For diode, capacitance is NOT constant under bias voltage

Capacitance

Definition of differential capacitance $$C = \left| \frac{dQ}{dV} \right|$$

At equilibrium: $$Q = eAN_A x_p = eAN_D x_n$$

Where: $$x_p = \frac{N_D}{N_D + N_A} W \quad ; \quad x_n = \frac{N_A}{N_D + N_A} W$$

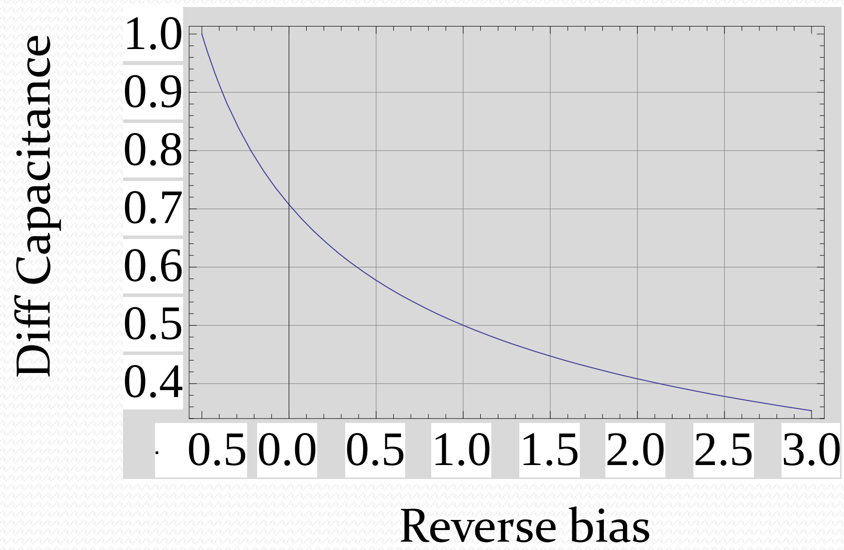
Capacitance (cont.)

$$x_p + x_n = W = \sqrt{\frac{2\varepsilon(V_o - V_b)}{e}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}$$

Hence:

$$C = \left|\frac{dQ}{dV}\right| = A\sqrt{\frac{N_D N_A}{N_D + N_A}}\sqrt{\frac{e\varepsilon}{2(V_0 - V_b)}}$$

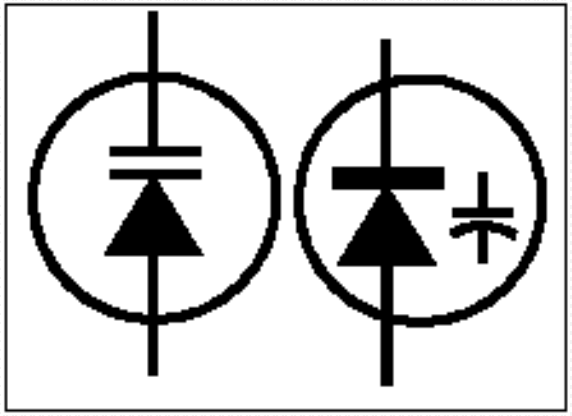
- This is typical behavior, BUT not unique. It applies to the simple case of uniform doping
- Different profiles are designed for special applications



More generally: $C \prec V^{-n}$

Example: varactors

- Specialized design for applications: VCO (voltage-controlled oscillators), amplifiers, tuners and frequency synthesizers, PLL (phase-locked loop).
- Non-constant doping profile
- Designed for range and voltage dependence behavior (power coefficient)
- Designed for high frequency applications (microwave)



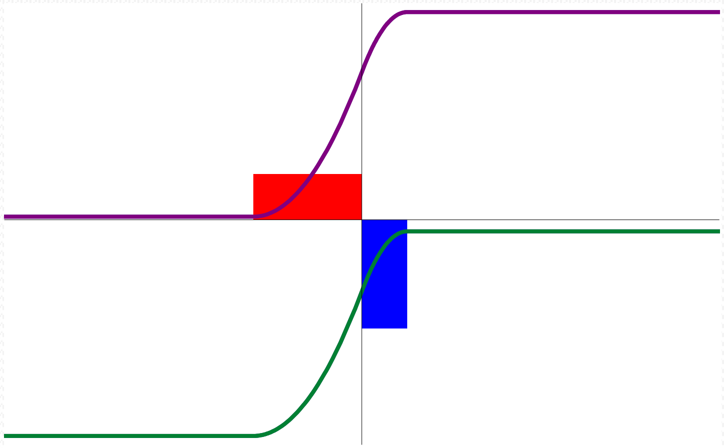
Modification of ideal diode behaviors

Three important regimes:

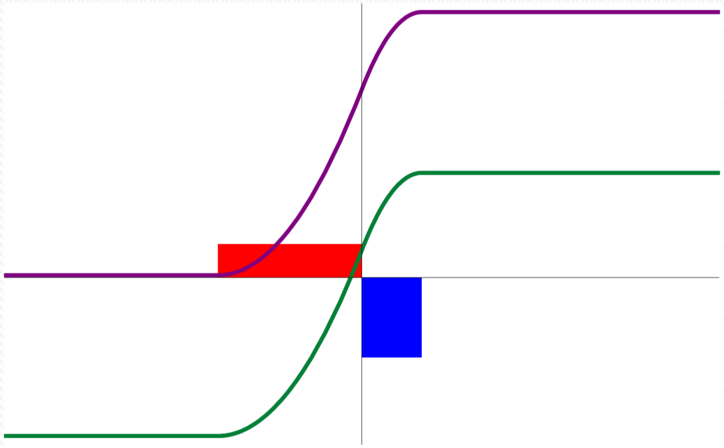
- Large forward bias (contact potential effect)
- Large reverse bias: reverse breakdown
- Highly non-symmetric diodes, long-based, short-based.

sense?

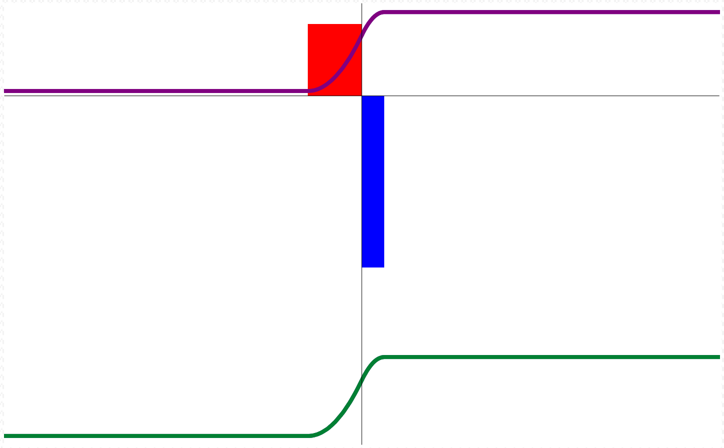
Zero bias



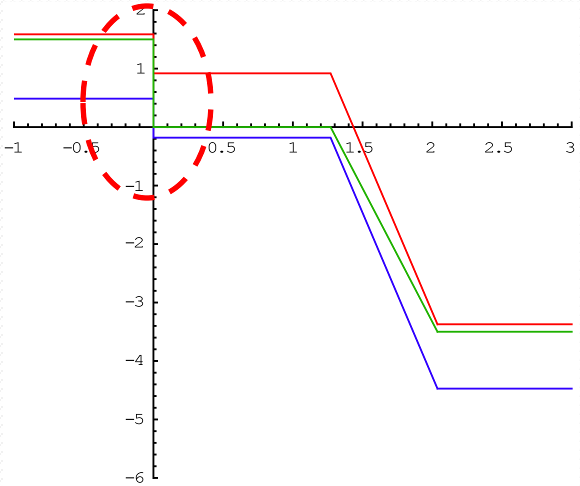
Reverse bias



Forward bias



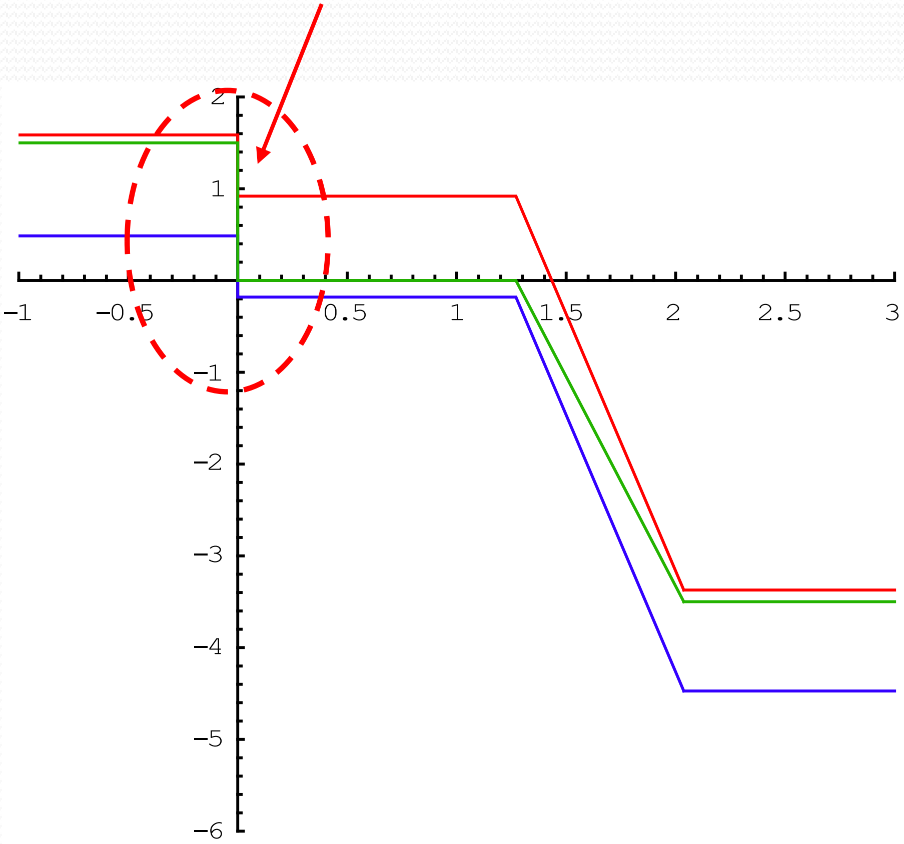
Very large forward bias



Contact potential effect

- A diode under a large forward bias voltage is a shorted-circuit device.
- The current theoretically goes to infinity (of course not in real life – because power supply fails before that
- Hence, the forward bias voltage cannot be increased arbitrarily large: clamping effect: or contact potential effect
- Forward bias voltage cannot exceed contact potential limit

This does NOT make sense (infinite E field, infinite current?)



Large forward bias

- With large forward bias and large current: excess minority currents are NOT negligible

Per charge neutrality

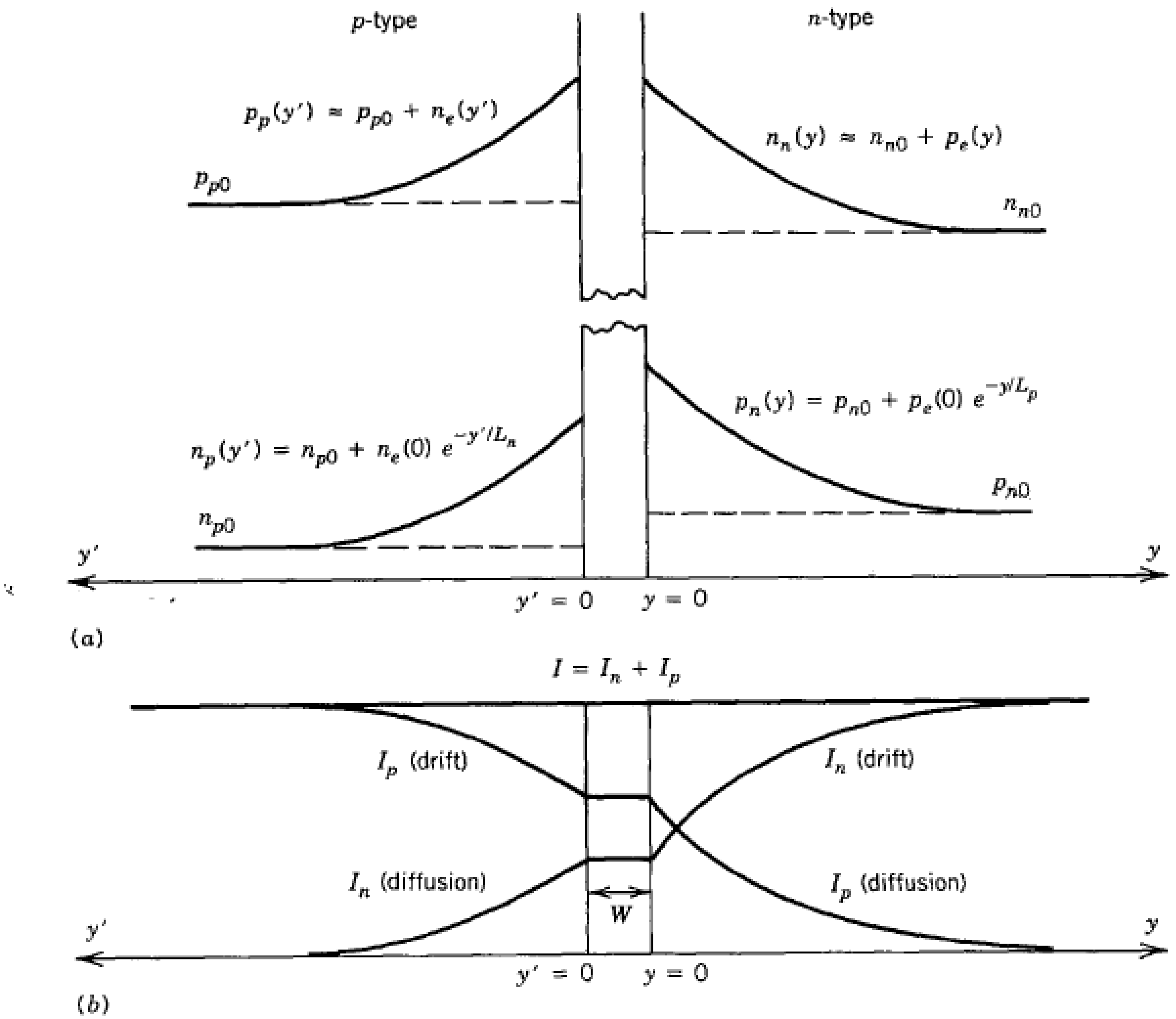
$$n_n = n_{no} + n_{ne} = n_{no} + p_{ne} \qquad p_p = p_{po} + p_{pe} = p_{po} + n_{ne}$$

Assuming Boltzmann distribution at large bias (Vb ~ Vo):

$$\frac{p_n}{p_p} \sim e^{-e(V_0 - V_b)/k_B T} \qquad \frac{n_p}{n_n} \sim e^{-e(V_0 - V_b)/k_B T}$$

Denote: $$e^{-e(V_0 - V_b)/k_B T} = e^{-\Delta E_b / k_B T}$$

Apply the same approach to obtain diffusion and drift current



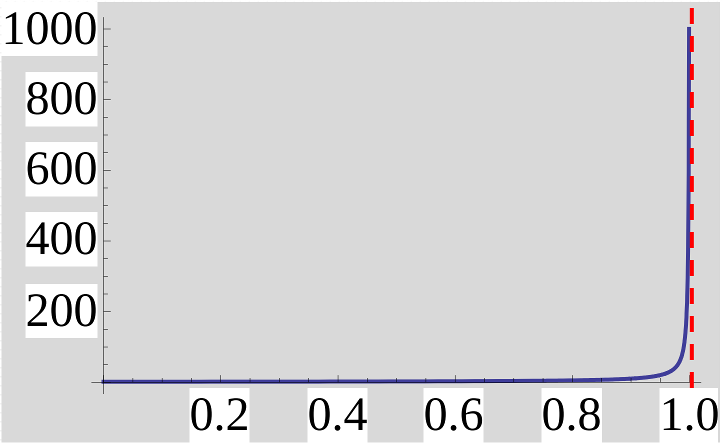
p-type
n-type
$p_p(y') \approx p_{p0} + n_e(y')$
p_{p0}
$n_n(y) \approx n_{n0} + p_e(y)$
n_{n0}
$p_n(y) = p_{n0} + p_e(0)\, e^{-y/L_p}$
$n_p(y') = n_{p0} + n_e(0)\, e^{-y'/L_n}$
p_{n0}
n_{p0}
y'
y
$y' = 0$
$y = 0$
(a)
$I = I_n + I_p$
I_p (drift)
I_n (drift)
I_n (diffusion)
I_p (diffusion)
W
y'
y
$y' = 0$
$y = 0$
(b)

Large forward bias (cont)

$$J \approx e n_i^2 \left(\frac{D_n}{L_n N_A} \left(1 + \frac{n_i^2}{n_n^2} e^{eV_b/k_BT} \right) + \frac{D_p}{L_p N_D} \left(1 + \frac{n_i^2}{p_p^2} e^{eV_b/k_BT} \right) \right) \left[e^{eV_b/k_BT} - 1 \right] \frac{1}{1 - e^{-2\Delta E_b/k_BT}}$$

Minority carrier currents

Contact potential



Contact potential

Large reverse bias

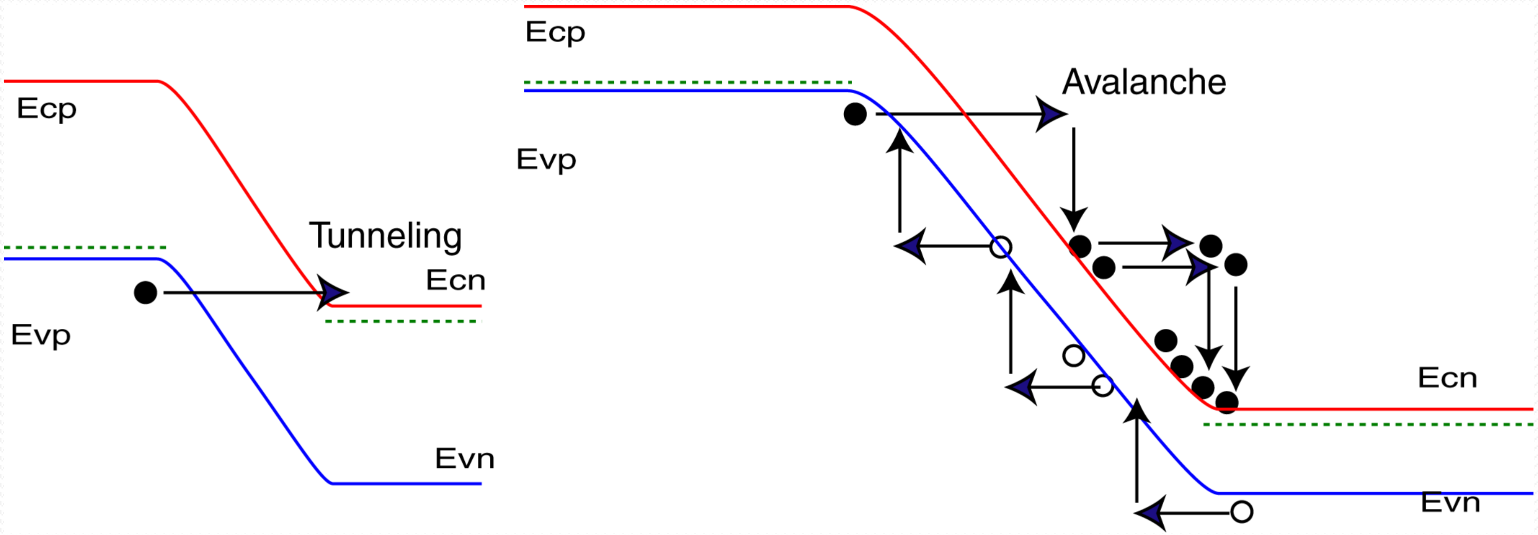
- Breakdown: Not the same as broken- although many diodes can be damaged with large reverse breakdown current
- A regime where simply the low voltage drift and diffusion current model is NOT sufficient
- Involve quantum tunneling effect and high field transport effects (non classical behaviors)

Large reverse bias (cont.)

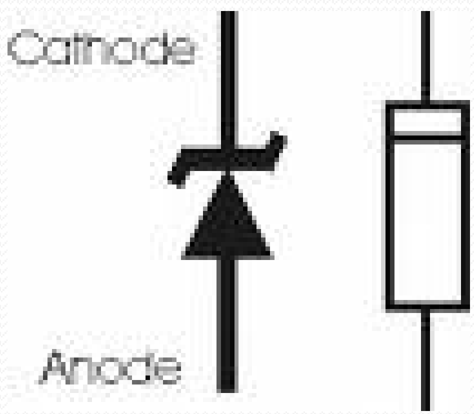
Two major effects:

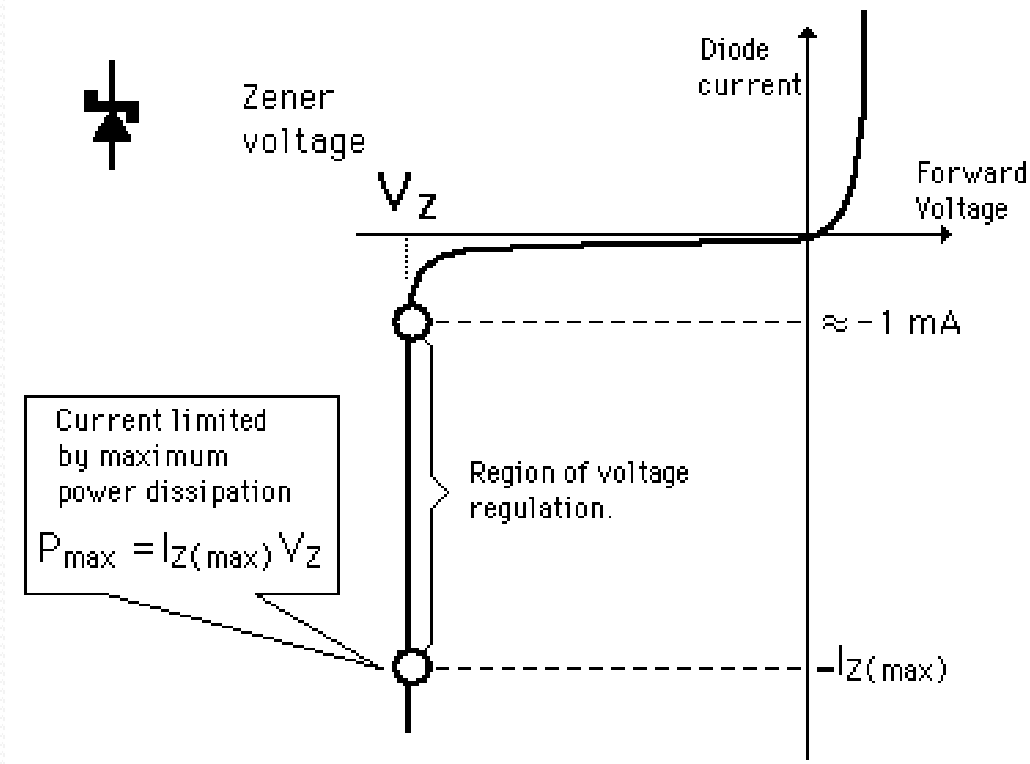
- Tunneling through the band; Zener
- Avalanche: impact ionization

Both are quantum mechanical effects – cannot be explained with classical transport. Tunneling involves coherent wavefunction: particles do not change energy in the process; avalanche is a relaxation process, particles lose energy to excite others.



Example: Zener diode



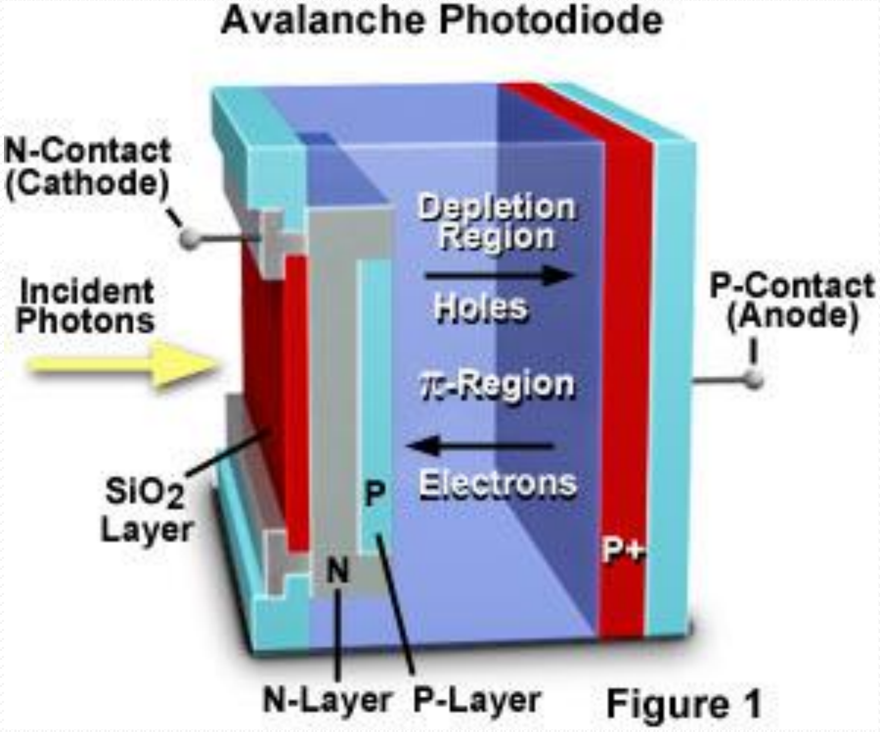


Usually designed with heavily doped junction

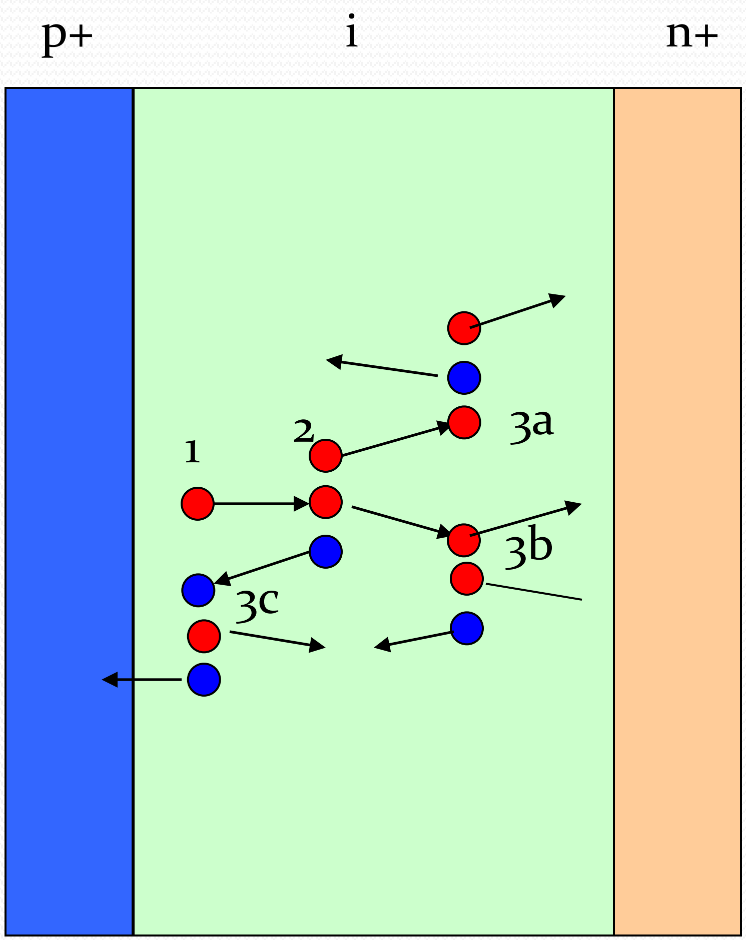
Example: avalanche diode

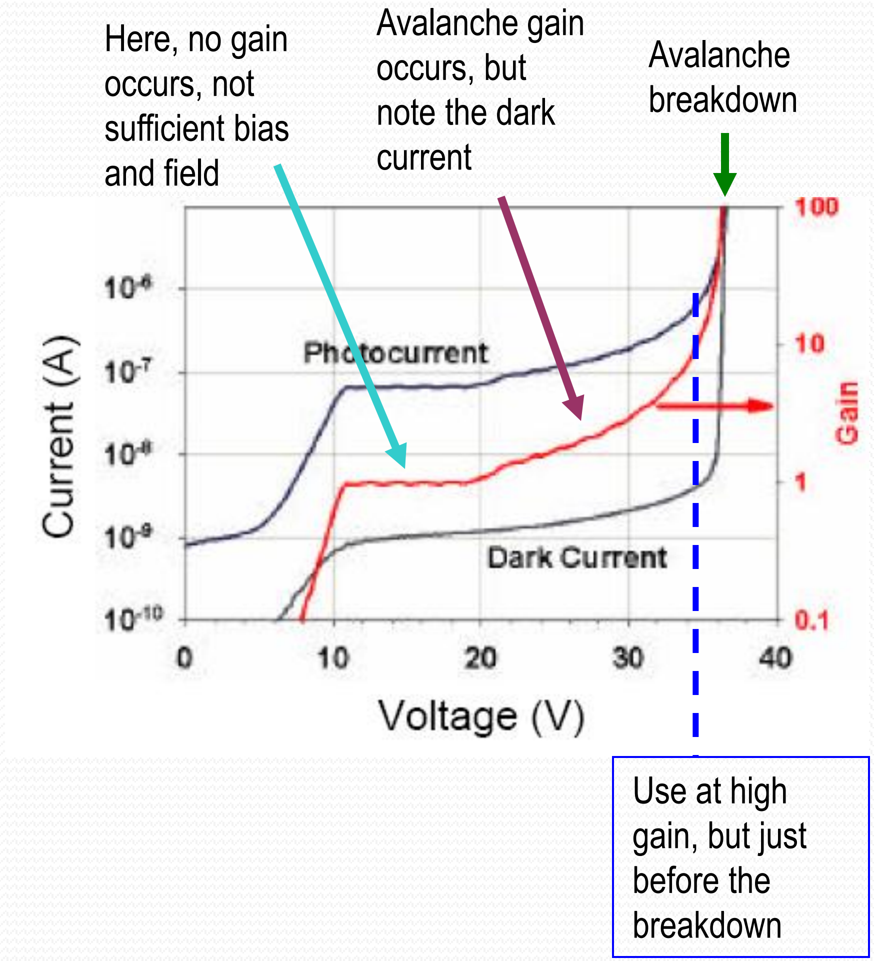
Avalanche region is undoped or very lightly doped (so as not to quench carriers)

One significant application is photodetection



Basics of PIN and APD





diode

- The diffusion model must take into account the geometry. The solution is not simply

  Exp[-x/L] but both Exp[-x/L] and Exp[x/L] with appropriate boundary conditions. Different diode transport behavior from ideal diode.
- The homework and case illustration is an example of highly asymmetric with very short p and long n.
- More example in bipolar junction transistors

Other junctions

- Heterojunction
- Schottky junction
- Ohmic junction

Junction fabrication

- Research paper