MOSFET – A Final Outlook

PROCESSORS microprocessors

Samsung teams with GlobalFoundries on 3D chips

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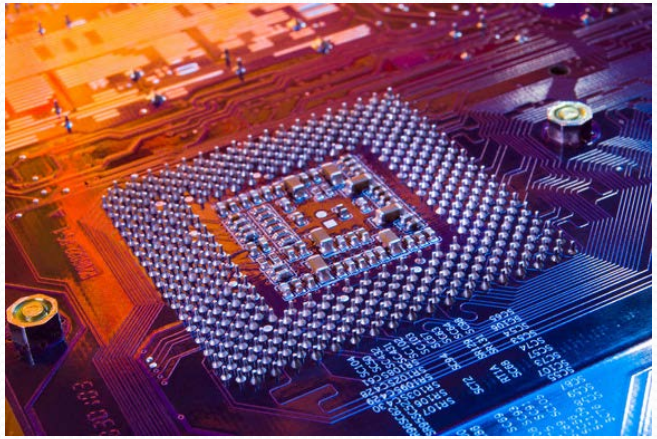


Samsung is partnering with chip manufacturer GlobalFoundries to increase the supply of low-power, high-speed chips for smartphones and tablets.

GlobalFoundries has licensed Samsung's 14-nanometer FINFET chip making process, which is used to manufacture 3D transistors. Those transistors will allow GlobalFoundries to make chips that are 20 percent faster and use 35 percent less power than chips made using its current 20-nanometer technology, the companies said.

GlobalFoundries doesn't use the chips itself. It's a foundry supplier, which means it makes chips for other companies that outsource their chip production, such as Advanced Micro Devices, Nvidia and Qualcomm.

Chip makers are constantly racing to build faster, more power-efficient chips, and the deal with Samsung will help GlobalFoundries compete better with other foundry suppliers such as Taiwan's TSMC.

In fact, GlobalFoundries had been pursuing its own 14-nanometer technology, which it planned to introduce this year. It has now dropped that technology, apparently deciding that Samsung's FINFET process is a better option.

Intel to make multi-die 14nm finfet devices with Altera

 richard wilson 28th March 2014

Altera and Intel are working together on the development of multi-die devices which integrate 14nm Stratix 10 FPGAs with memory, processors and analogue components in a single package.

The heterogeneous multi-die devices incorporate 3D silicon technology and Intel's 14nm Tri-Gate (finfet) process technology.

Intel is already manufacturing Altera's Stratix 10 FPGAs and system-on-chip devices (SoCs) using the 14nm Tri-Gate process.

Intel and Altera are currently developing test vehicles aimed at streamlining manufacturing and integration flows.

"Our partnership with Altera to manufacture next-generation FPGAs and SoCs using our 14nm Tri-Gate process is going exceptionally well," said Sunit Rikhi, vice president and general manager, Intel Custom Foundry.

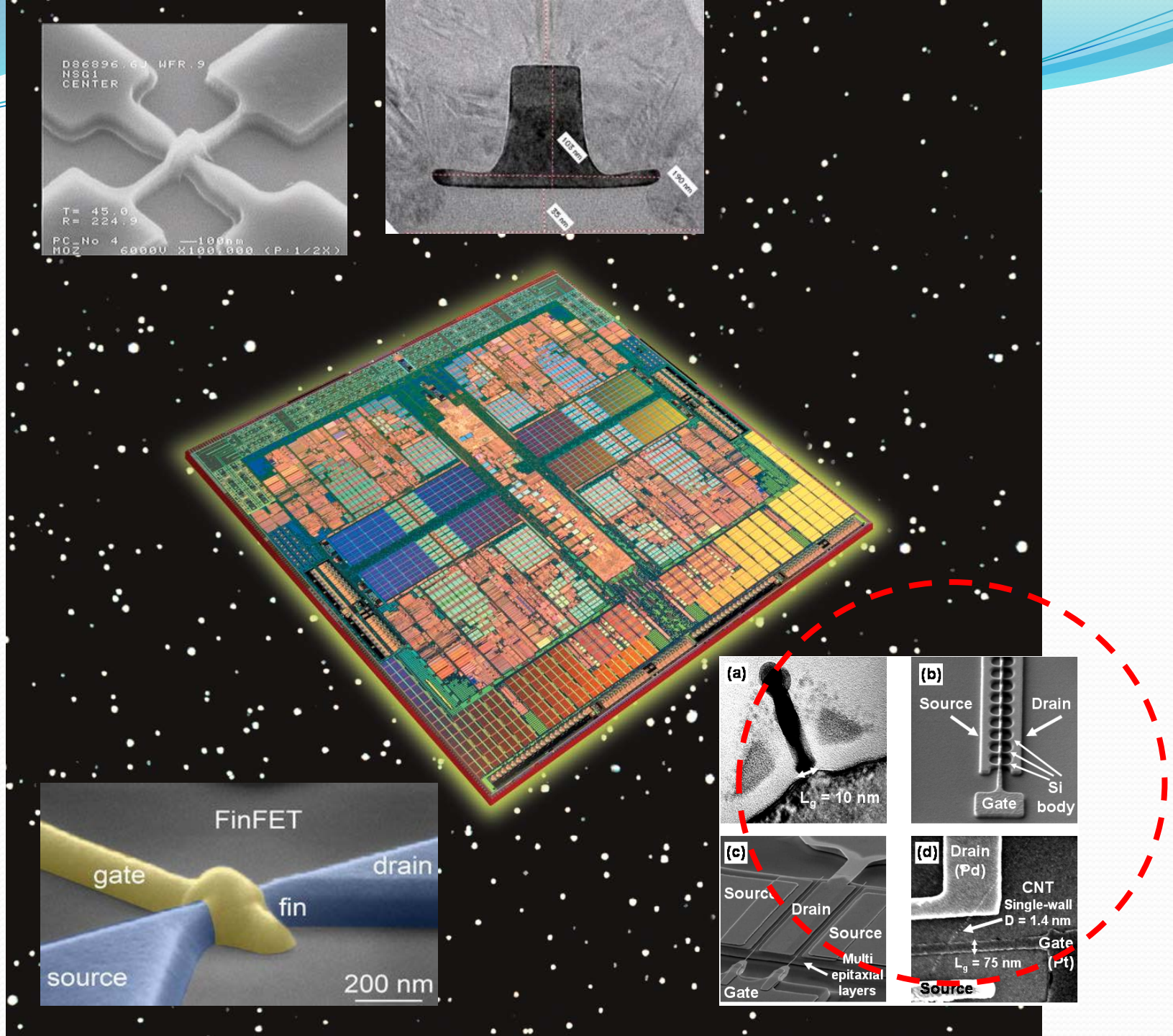
"Our close collaboration enables us to work together in many areas related to semiconductor manufacturing and packaging," said Rikhi.

Together, both companies are building off one another's expertise with the primary focus on building industry-disrupting products."

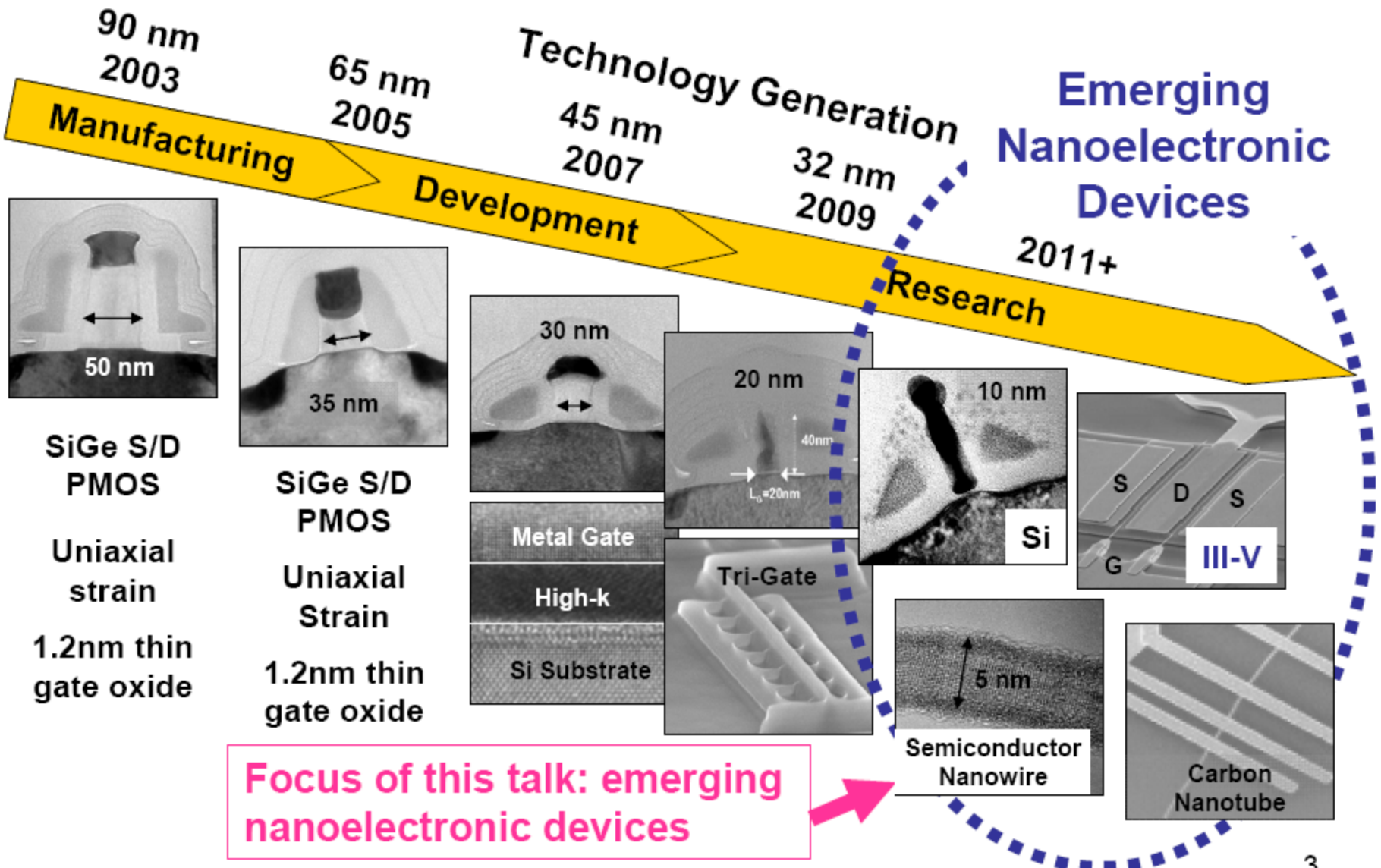
According to Brad Howe, senior vice president of R&D at Altera, access to Intel's manufacturing and chip packaging capabilities is allowing the FPGA supplier to offer system-in-a-package products which are "critical to meeting overall performance requirements."

Related news:

Altera: 14nm Stratix and 20nm Arria FPGA details


D86896.6U WFR.9
NSG1
CENTER
T= 45.0
R= 224.9
PC_No 4 100nm
MOZ 6000V X100,000 (P:1/2X)
FinFET
gate
drain
fin
source
200 nm
(a)
L_g = 10 nm
(b)
Source
Drain
Si body
Gate
(c)
Source
Drain
Source
Multi epitaxial layers
Gate
(d)
Drain (Pd)
CNT
Single-wall
D = 1.4 nm
Gate (Pt)
L_g = 75 nm
Source

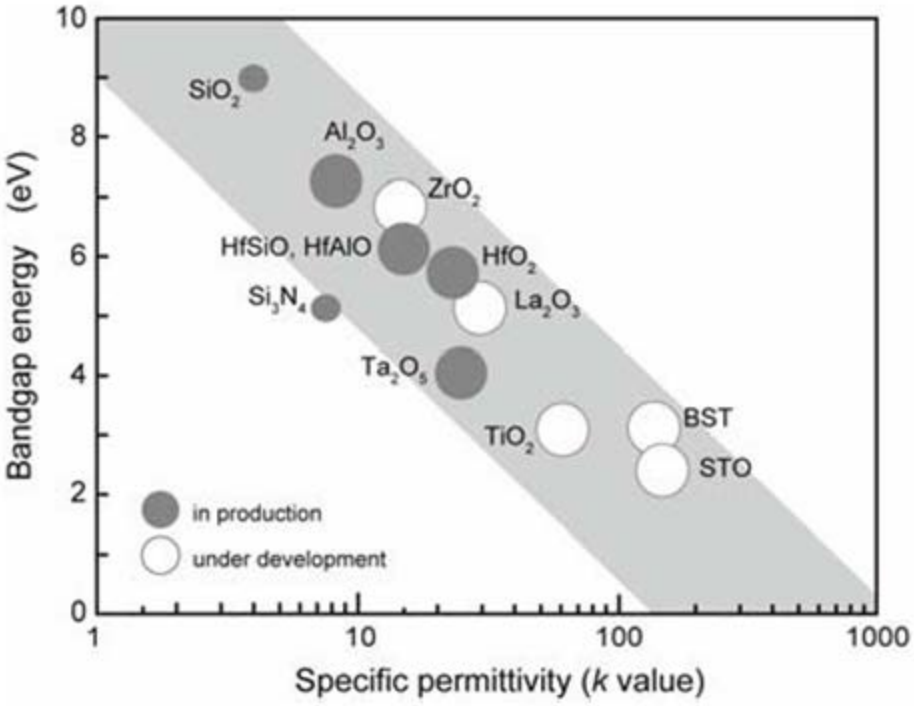
Transistor Nanotechnology

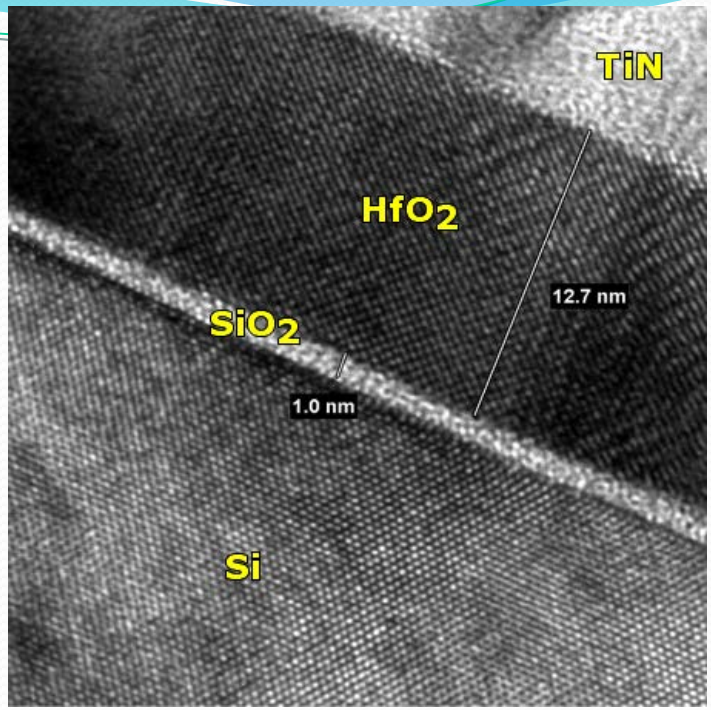


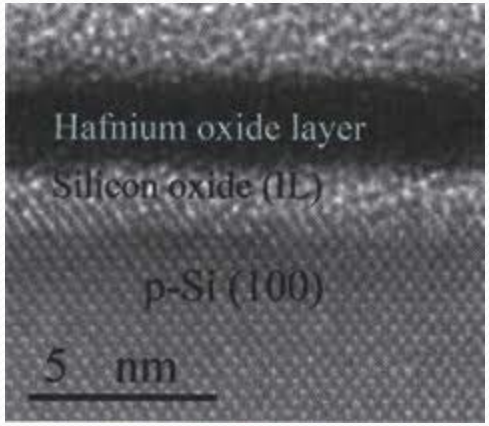
Source: Robert Chau, Intel

Note: Future options subject to change


Moore's Law Requires More Than Just Scaling
130nm
2001
Scaling
Scaling
Materials Science
90nm
2003
65nm
2005
45nm
2007
32nm
2009
22nm
2011
www.semiaccurate.com
Strained Silicon >3yrs
1st Competitor
S|A
High-k Metal Gate >3.5yrs
1st Competitor
Tri-Gate 4yrs?

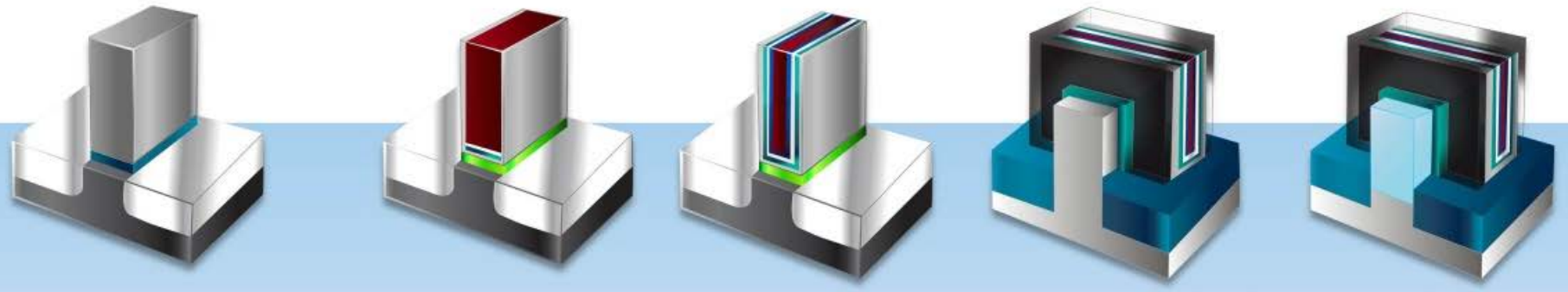

Bandgap energy (eV)
Specific permittivity (k value)
SiO2
Al2O3
ZrO2
HfSiO, HfAlO
HfO2
Si3N4
La2O3
Ta2O5
TiO2
BST
STO
in production
under development
0
2
4
6
8
10
1
10
100
1000


TiN
HfO2
SiO2
12.7 nm
1.0 nm
Si


Hafnium oxide layer
Silicon oxide (IL)
p-Si (100)
5 nm

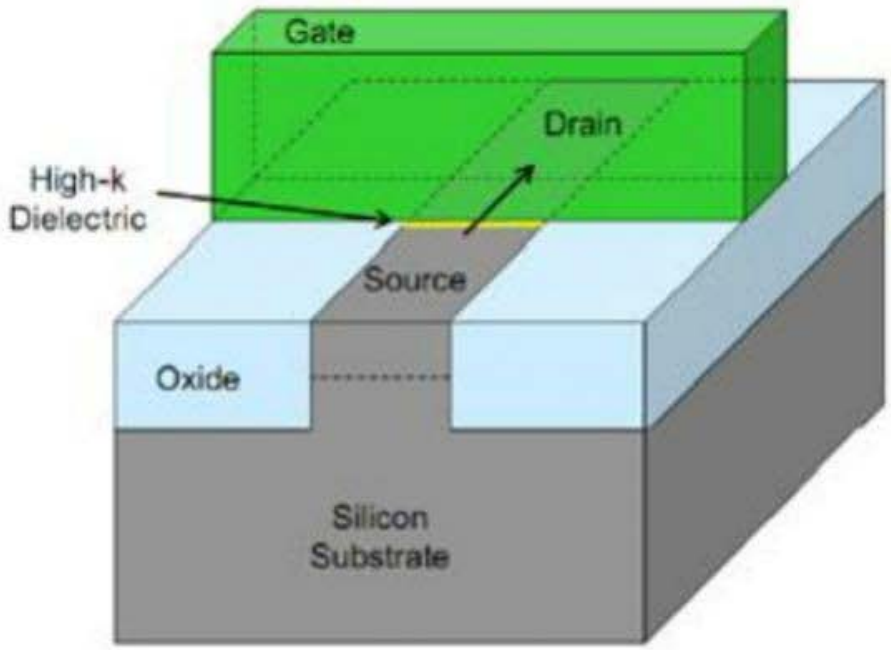
The TRANSISTOR Evolution

APPLIED MATERIALS®



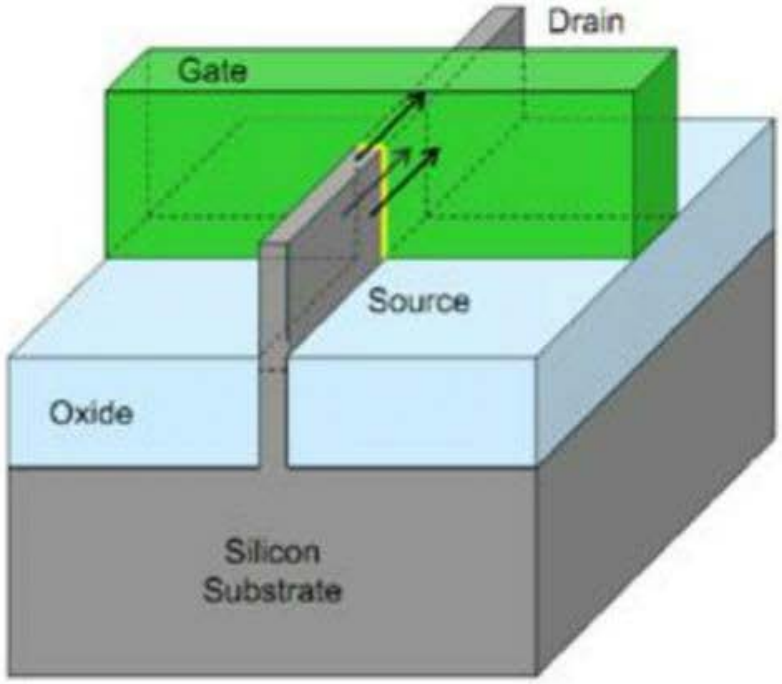
High Performance Low Power Transistors Enabled By Innovations in Device Architecture & Process Technologies

Traditional Planar

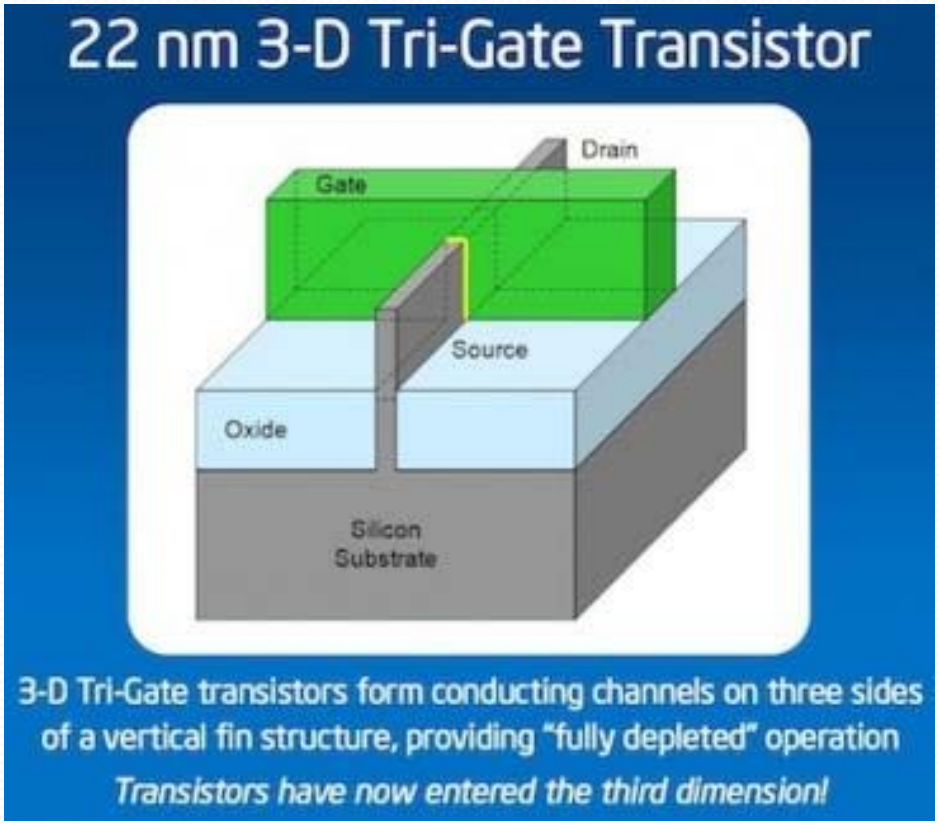


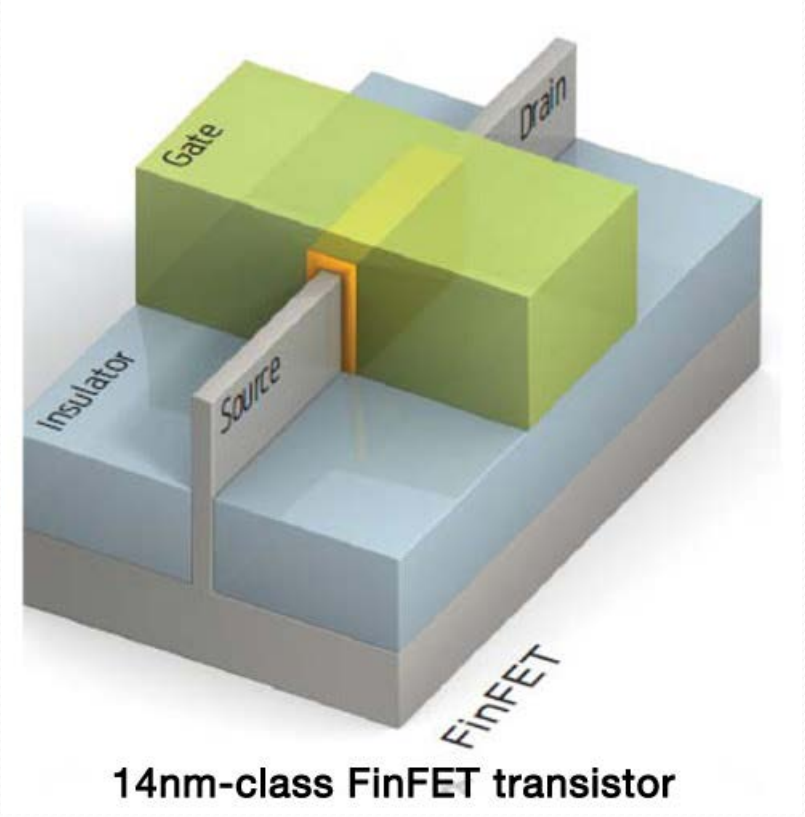
Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

3D FinFET

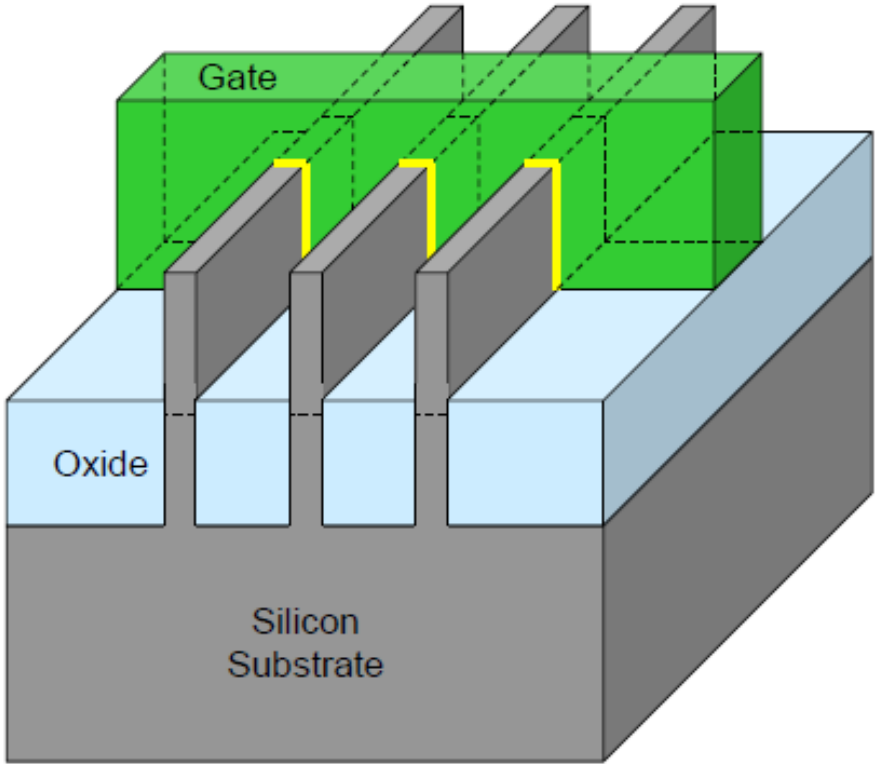


3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

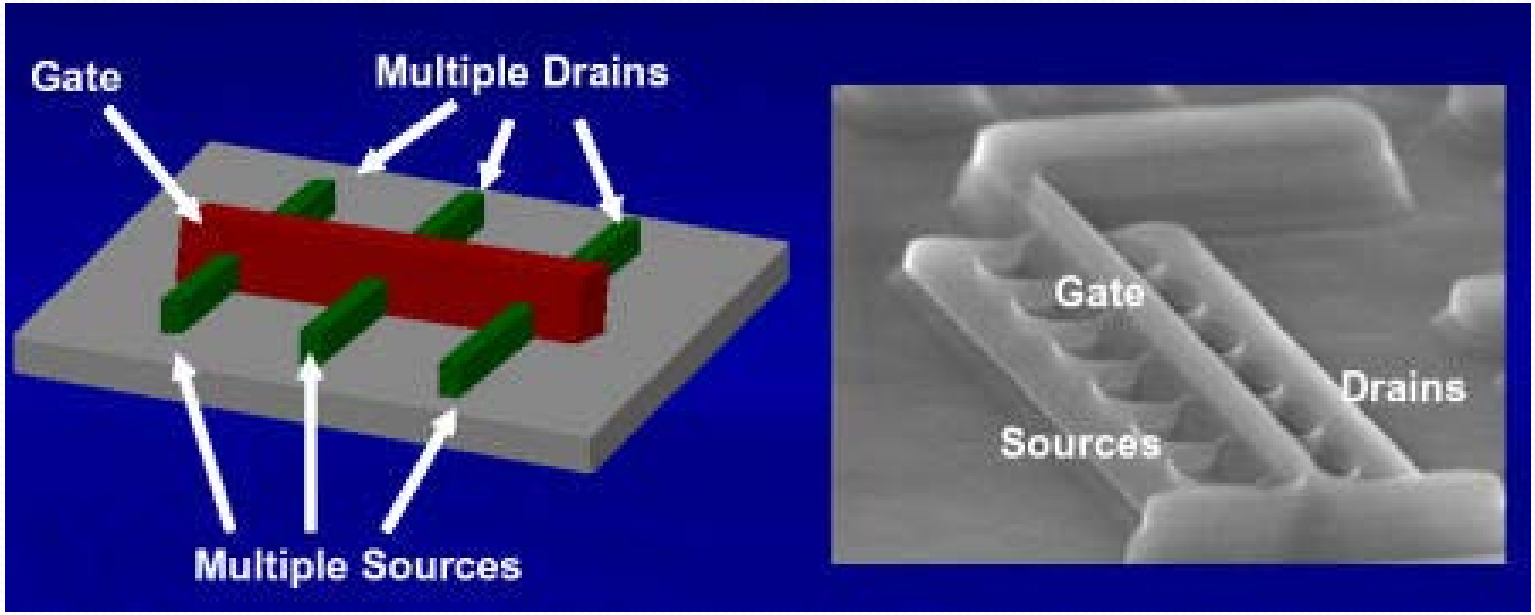

22 nm 3-D Tri-Gate Transistor
Drain
Gate
Source
Oxide
Silicon
Substrate
3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation
Transistors have now entered the third dimension!


Gate
Drain
Insulator
Source
FinFET
14nm-class FinFET transistor

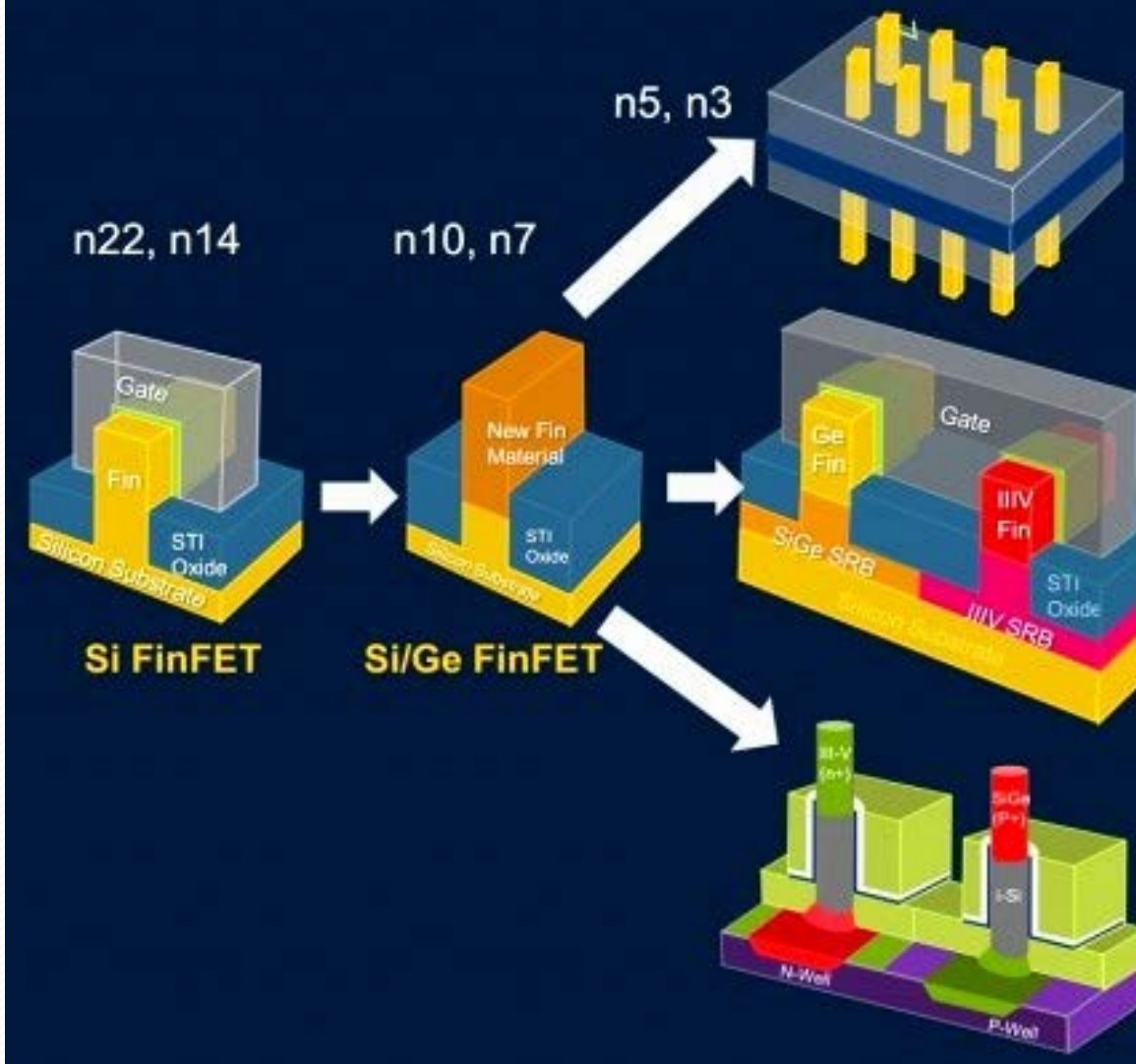
22 nm Tri-Gate Transistor



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance


Gate
Multiple Drains
Multiple Sources
Gate
Drains
Sources

Transistor Pathway



Si/Ge Gate All Around (GAA)
Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

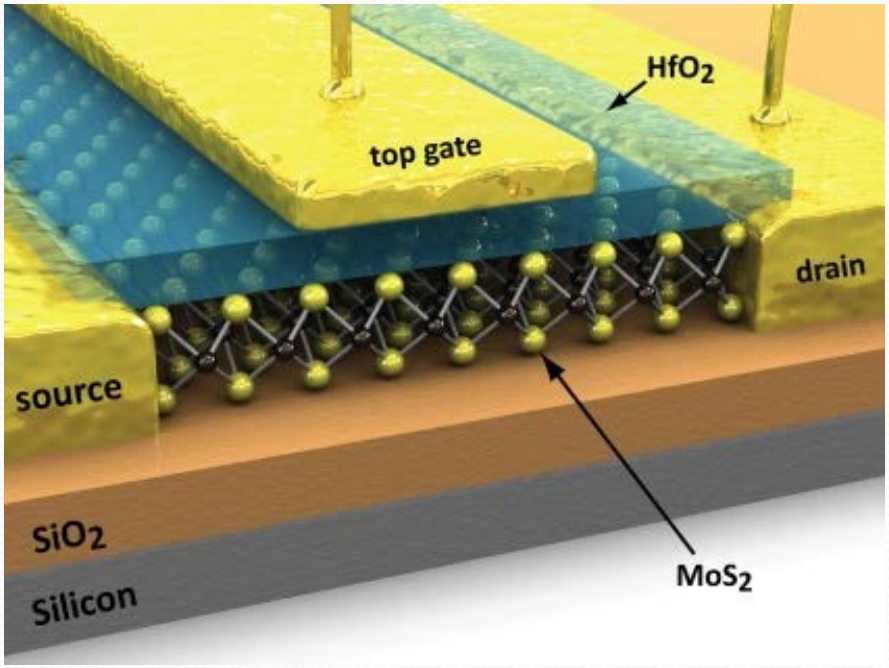
III-V FinFET

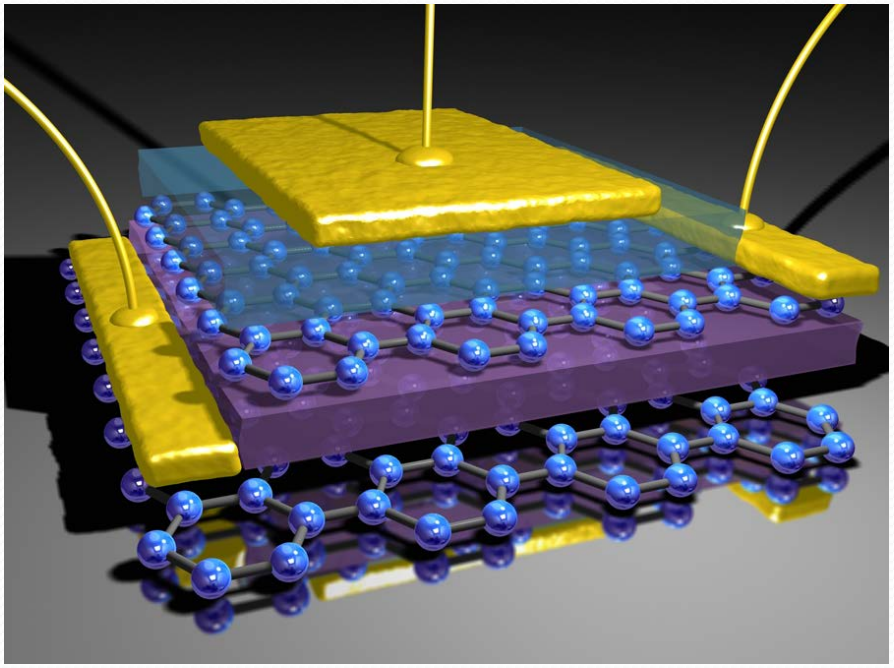
Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

Vertical TFET

Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP

Non-Conventional Channel Materials?





Molybdenum Disulfide

Graphene

See http://spectrum.ieee.org/nanoclast/semiconductors/materials/cause-of-2d-molybdenum-disulfides-electronic-shortcomings-revealed

Roadmap to the future