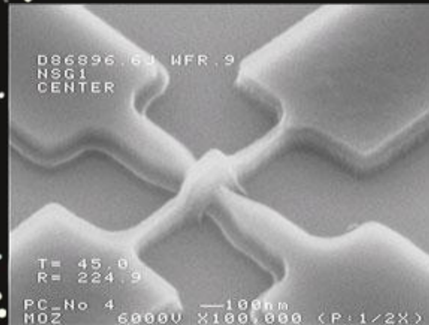
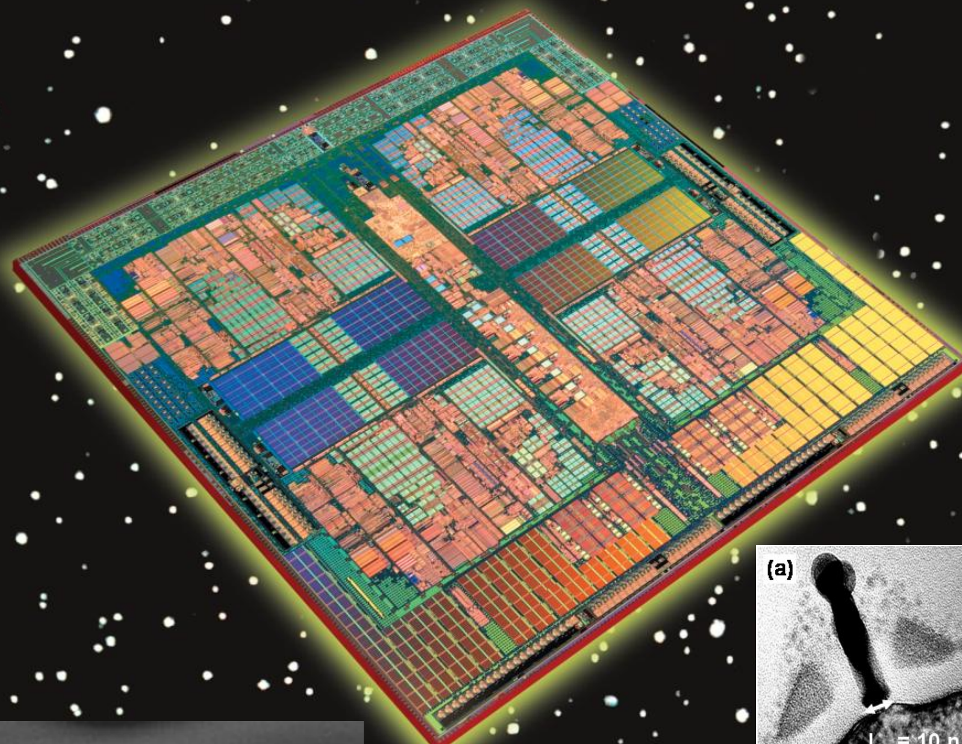
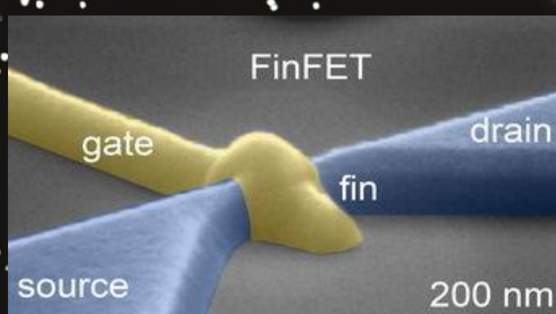
Field-Effect Transistors

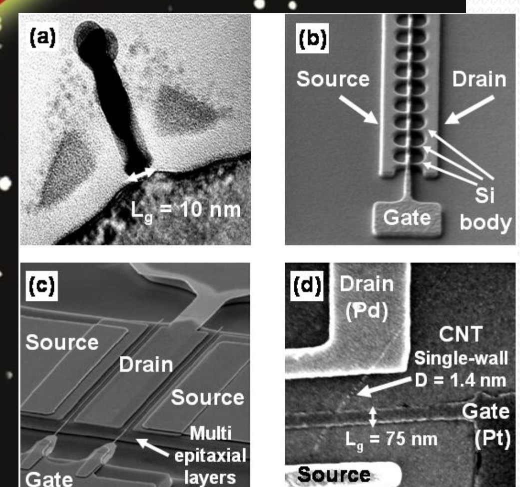
Outline

- Introduction to transistor & FET (vs BJT)
- Basic aspect of MOSFET
- MOSFET operations & models
- MOSFET technology
- Other FET technology

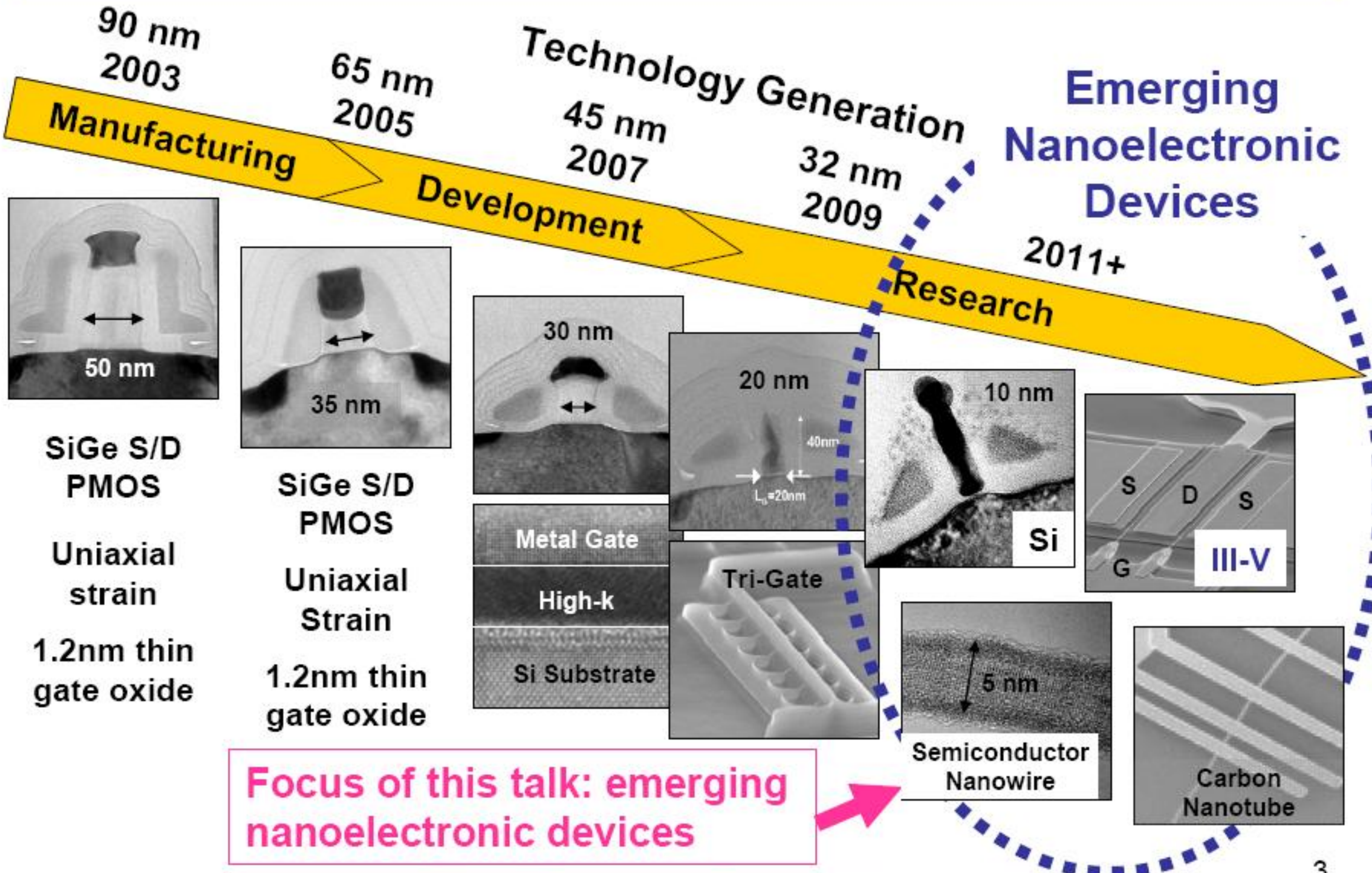

D86896.6J WFR.9
NSG1
CENTER
T= 45.0
R= 224.9
PC_No 4 100nm
MOZ 6000V X100,000 (P:1/2X)




FinFET
gate
drain
fin
source
200 nm


(a)
L_g = 10 nm
(b)
Source
Drain
Si body
Gate
(c)
Source
Drain
Source
Multi epitaxial layers
Gate
(d)
Drain (Pd)
CNT Single-wall D = 1.4 nm
Gate (Pt)
L_g = 75 nm
Source

Transistor Nanotechnology

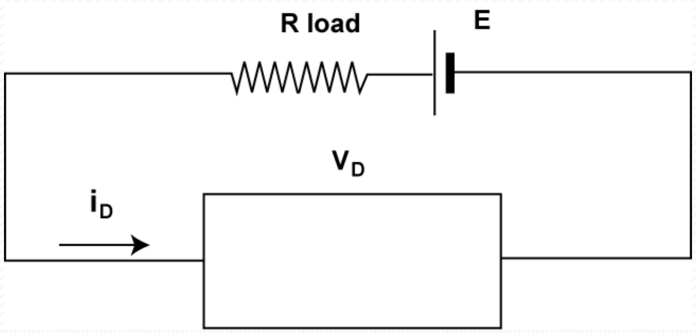


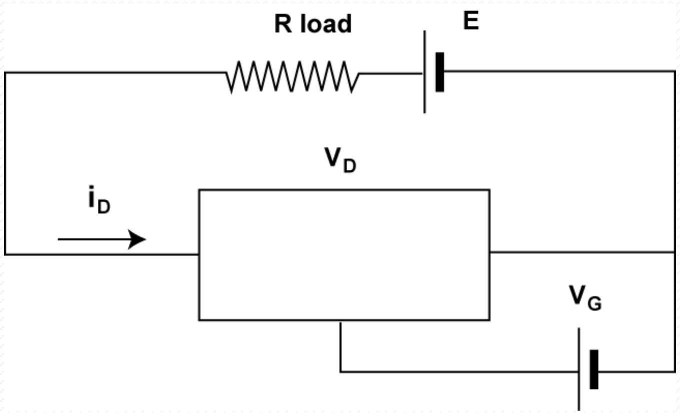
Source: Robert Chau, Intel

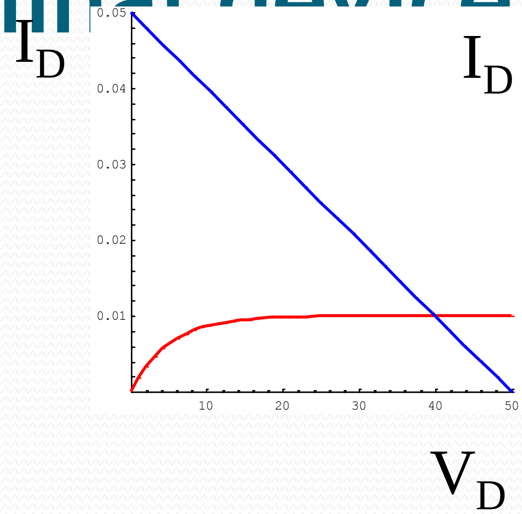
Note: Future options subject to change

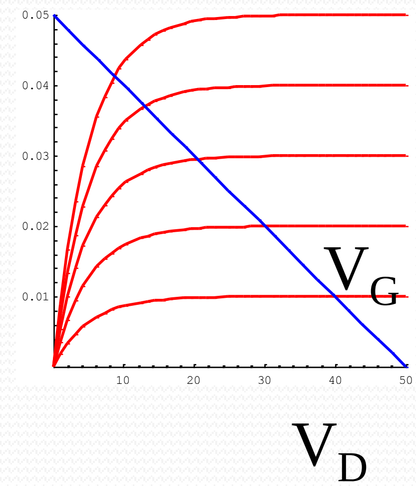
What is Field Effect Transistor?

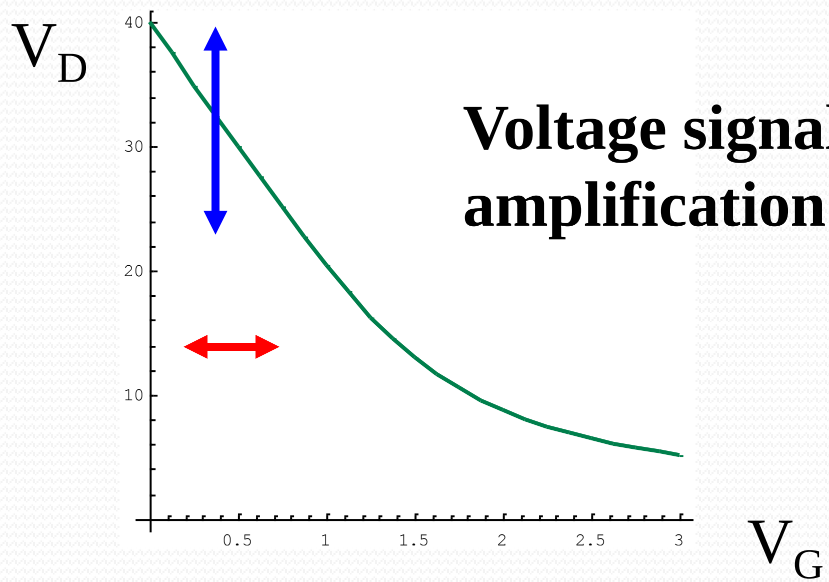
Transistor: a 3-terminal device





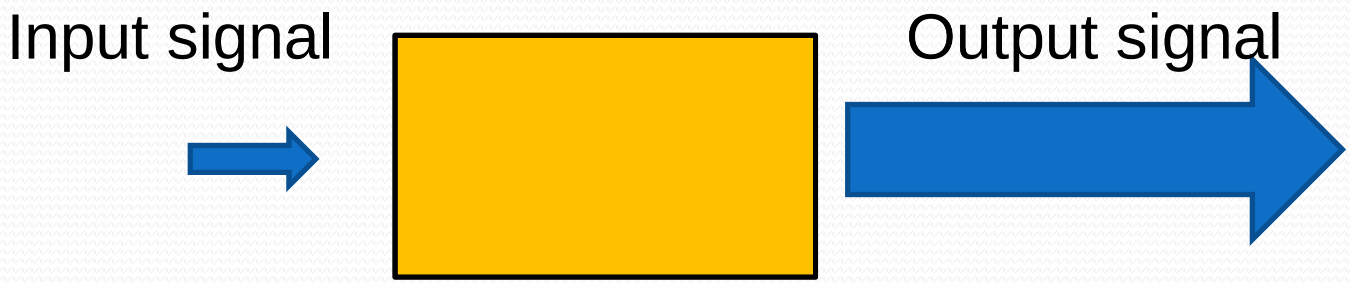






Voltage signal amplification

Elementary Concept of Amplification



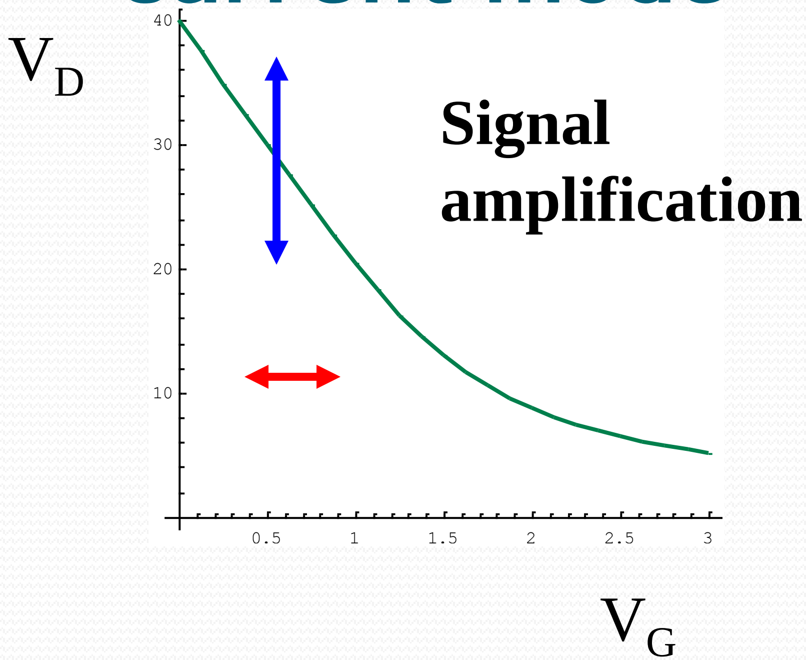
The key physical quantity is Power

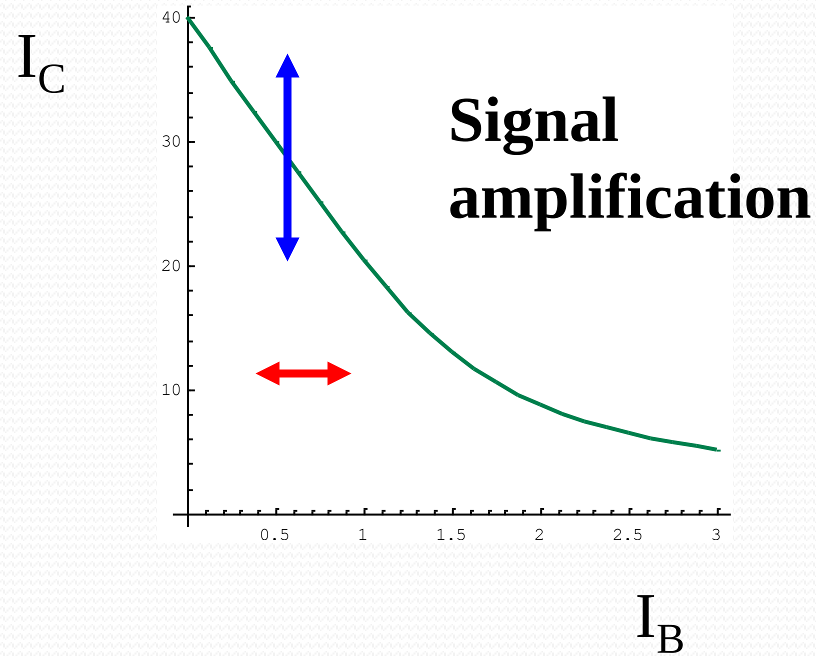
Power = V x I

Any amplifier or switching device must operate on:

- Either voltage
- Or current

Signal control in voltage mode or current mode





Voltage control

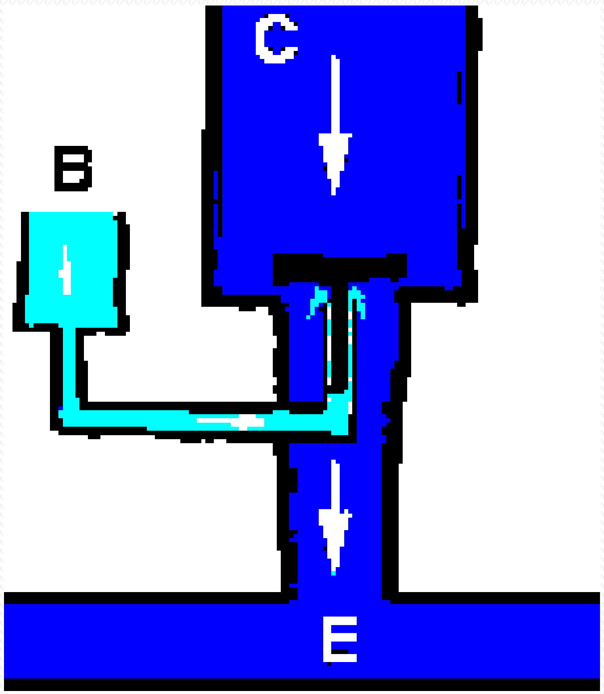
Electric field (at the gate) is the “lever”

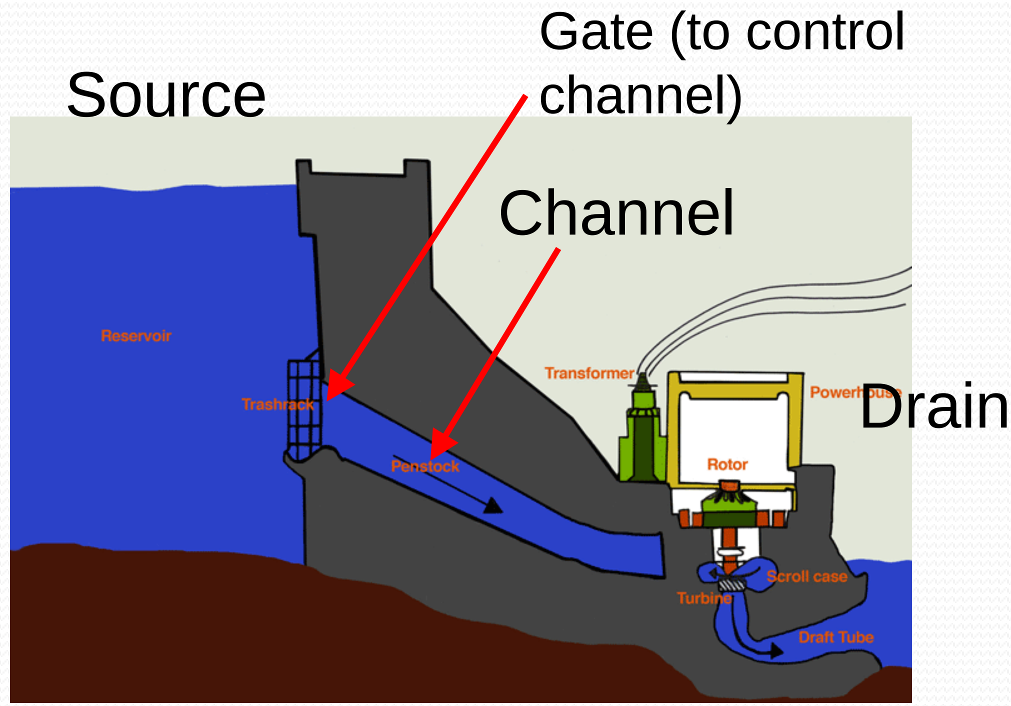
→ Field-effect transistor

Current control

Injected (base) current is the “lever”

→ Bipolar junction transistor





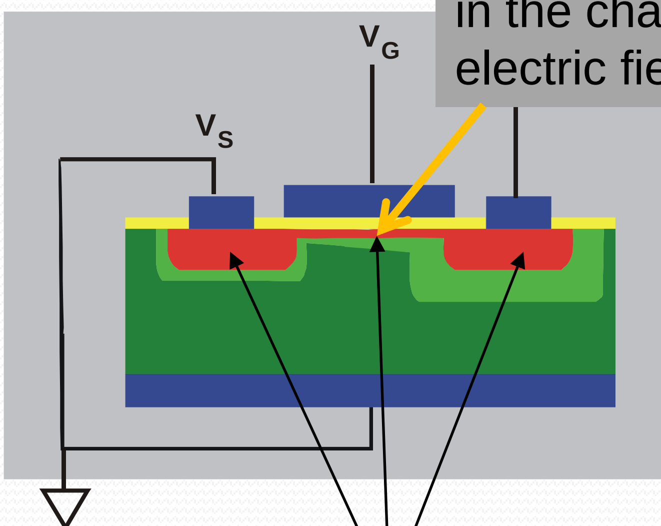
small power to control a large power

FET and BJT

An comparative overview

The key difference between FET and BJT

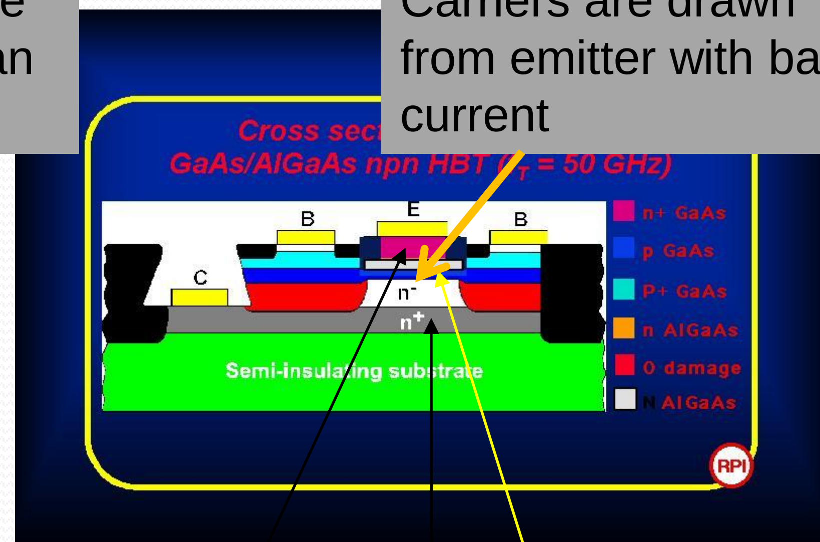
FET



Carriers are generate in the channel with an electric field (gate)

Same type of carriers in source, drain, channel

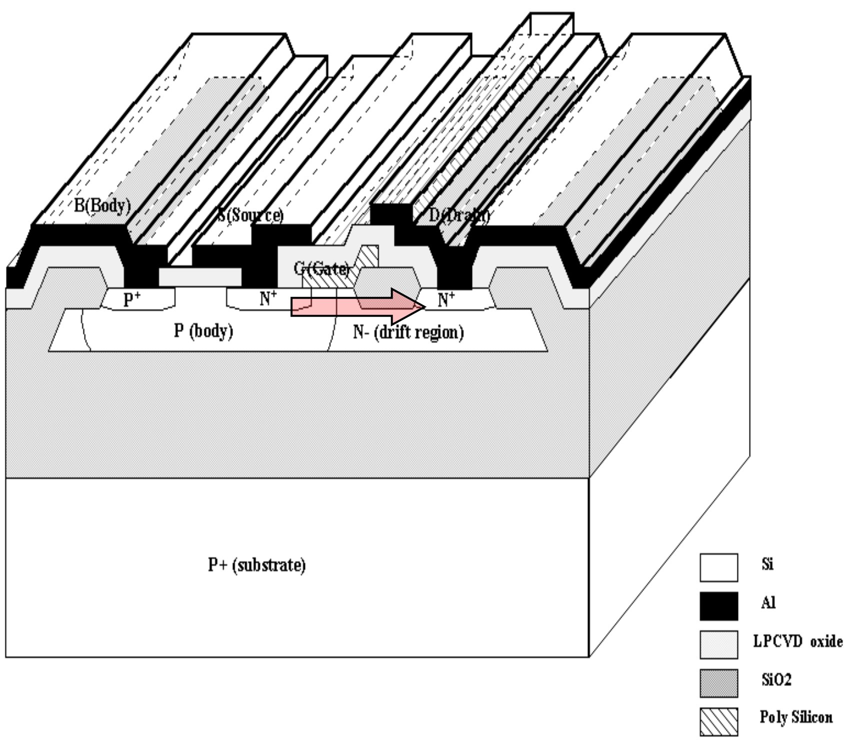
BJT

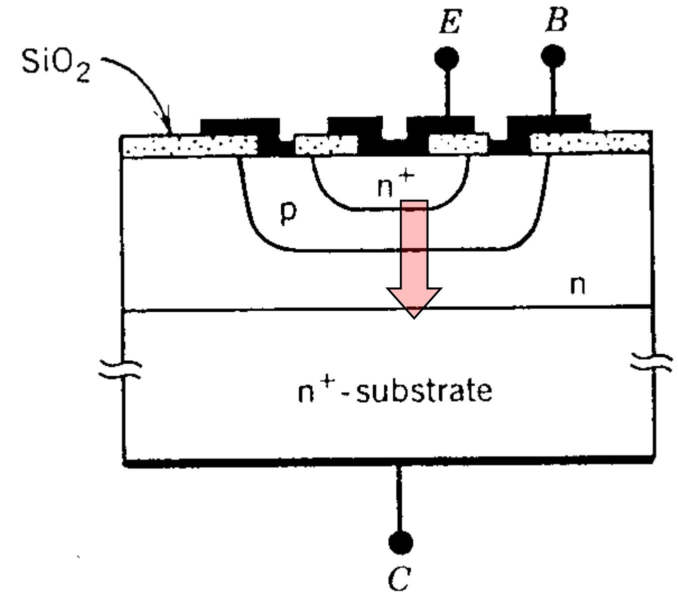


Carriers are drawn from emitter with base current

Same type of carriers for emitter and collector, opposite type for base

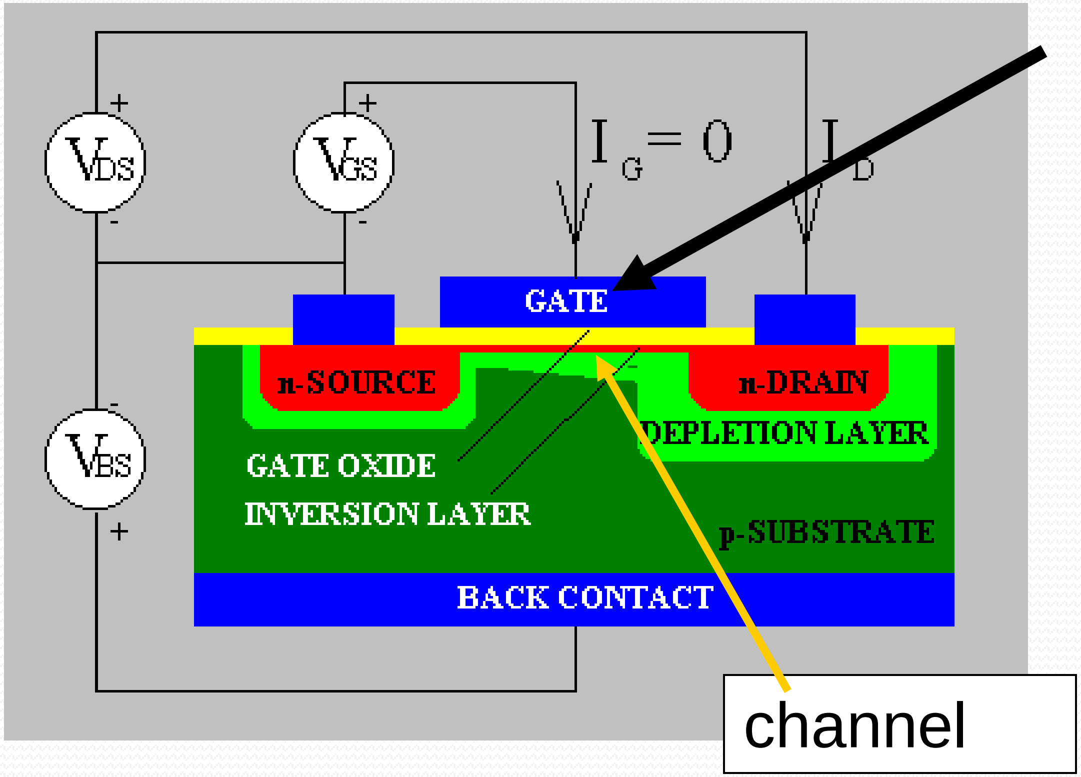
FET vs BJT
lateral vs planar (usually)





What is field-effect?

A device in which the main action (amplification, attenuation, switching,…) is controlled by externally applied electric field



This gate can open or shut carrier flow between the source and drain: An electric field can open or close a channel

Physics of MOSFET Channel

How do you create a “river of electrons” in a “land of holes”? And vice versa

Consider…

- An intrinsic semiconductor has no dominant carrier type
- It can be p-doped or n-doped
- It can be reversed p-type or n-type with opposite doping (n-dope in p-type and p-dope in n-type)
-… but most remarkably: it can have conducting electrons in p-type and vice versa… known as “inversion”

Why field-effect?

Field control:

• very small current required

• high impedance

• low power required for switching

• suitable for lower power signal processing, logic operation

Current control:

• some current required

• lower impedance

• required some power for switching

• suitable for power amplification, analog signal processing

Key concepts in FET

Source

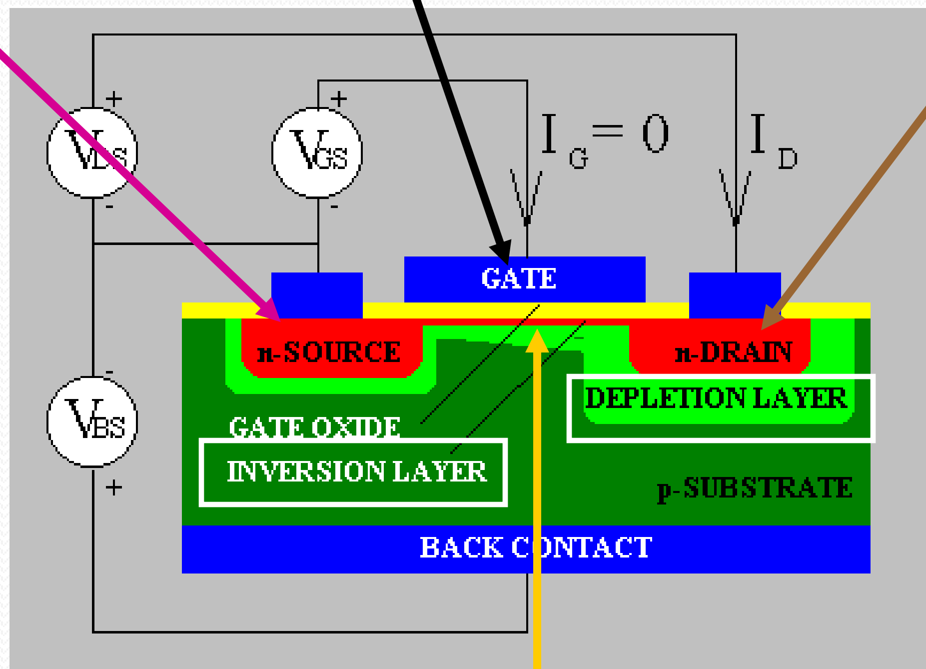
High carrier density region

Gate

Induce an electric field on the channel

Drain

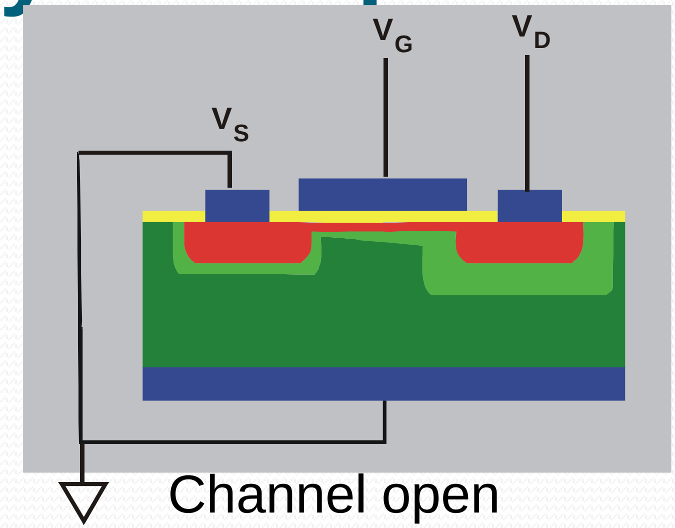
End collection for carrier



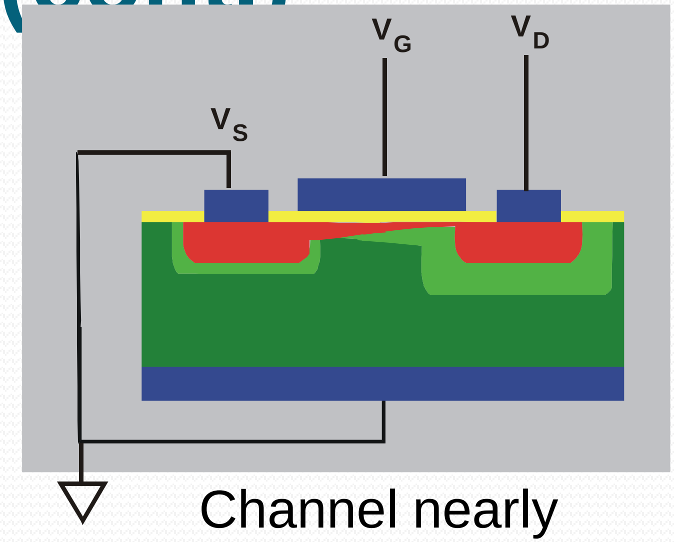
Channel

A “river” of carriers in a region of opposite carriers

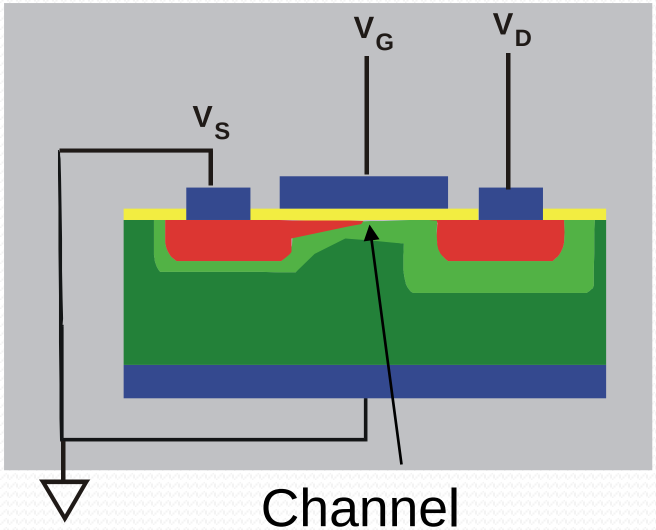
Key concepts in FET (cont.)



Channel open



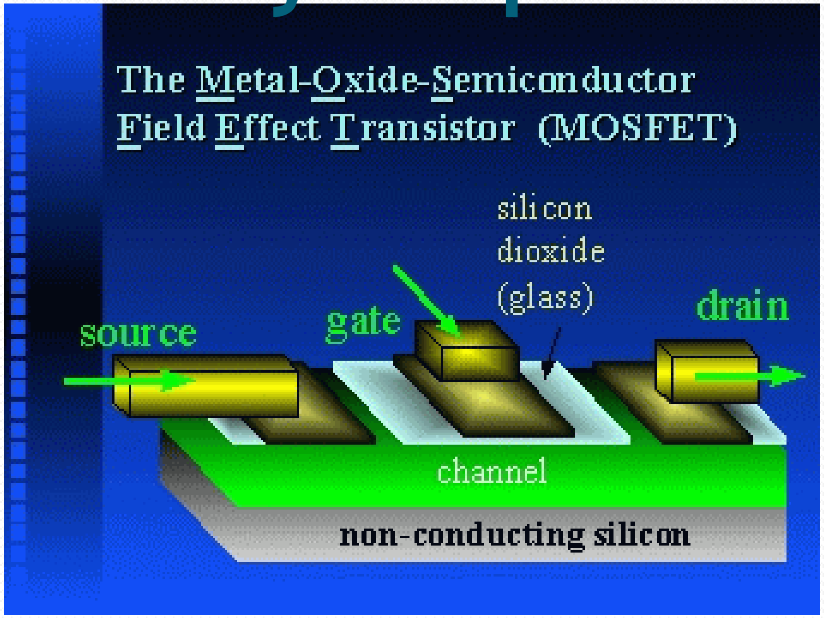
Channel nearly close

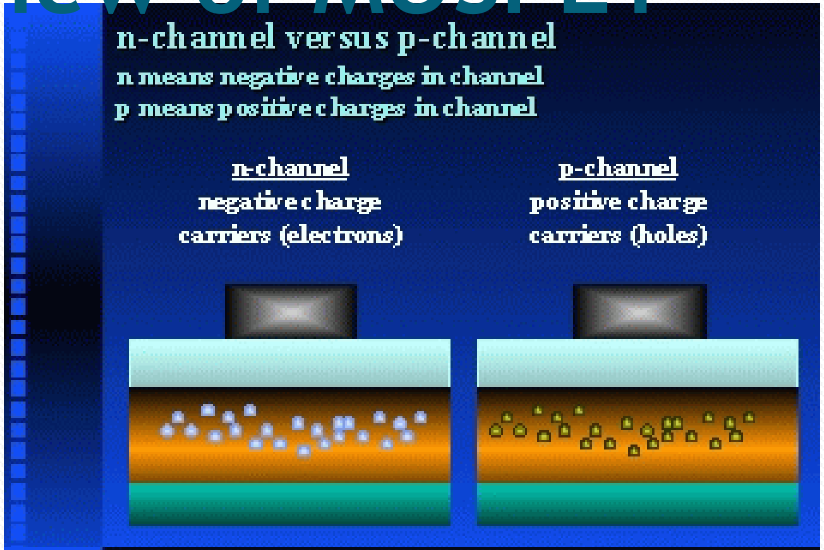


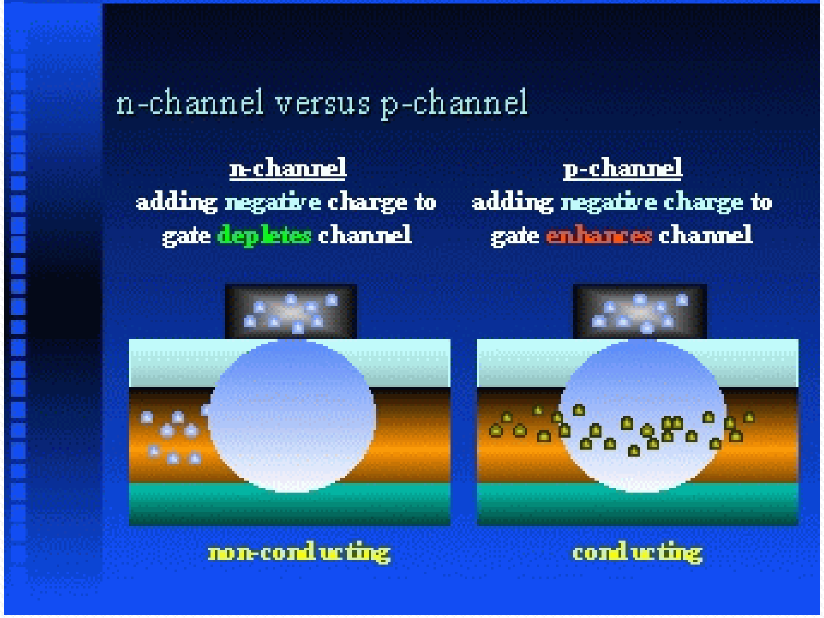
Channel pinched-off

- What is a channel? How is it formed?
- What is a pinch-off? How does it happen?
- How does a channel control the current flow between source and drain?

A very simplistic view of MOSFET







“Generic” FET

- What is a channel?

A region that conducts electricity between the source and drain, of which, the conductivity (or differential resistance) can be controlled by an external voltage, called gate voltage.

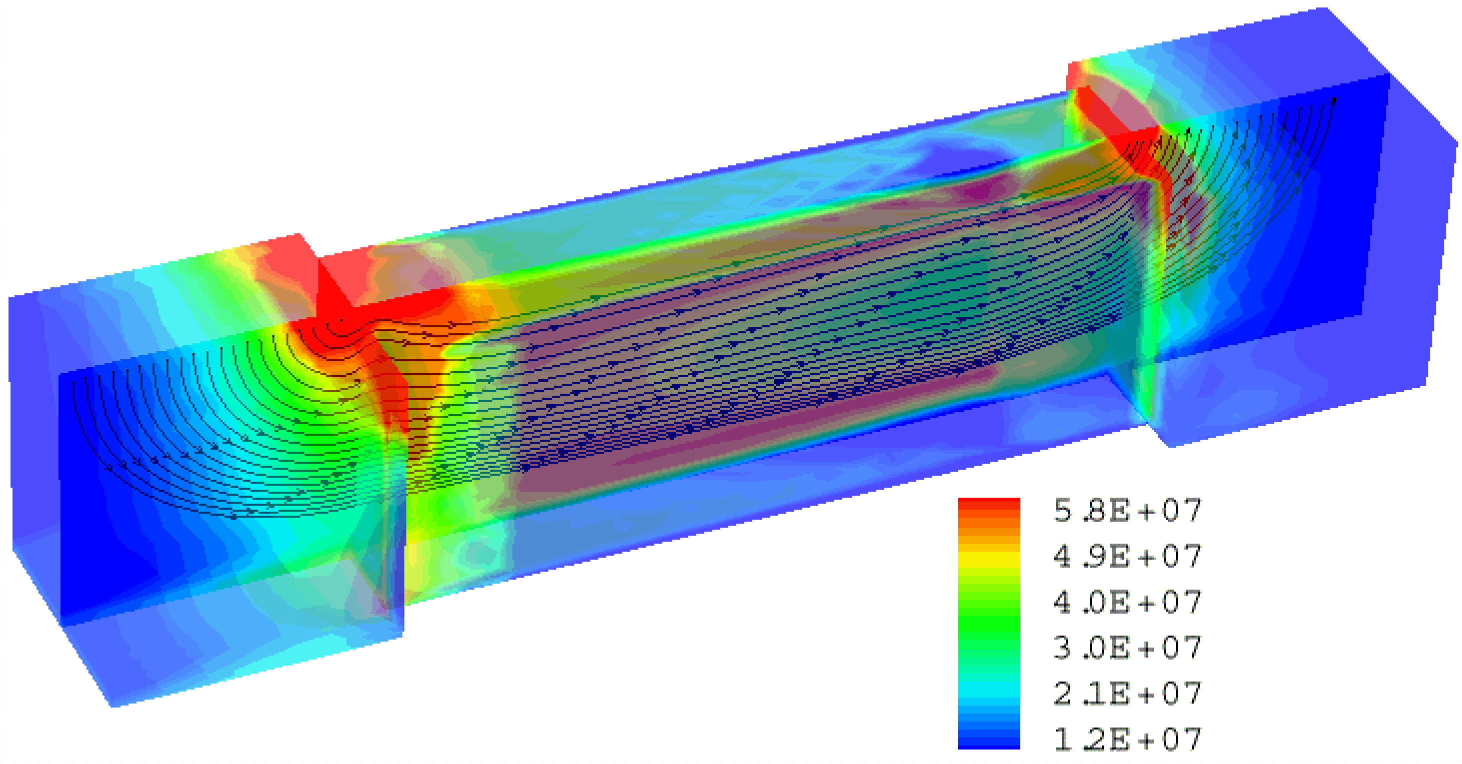
- How is it formed?

- a doped region of a semiconductor (direct doping, modulation doping)

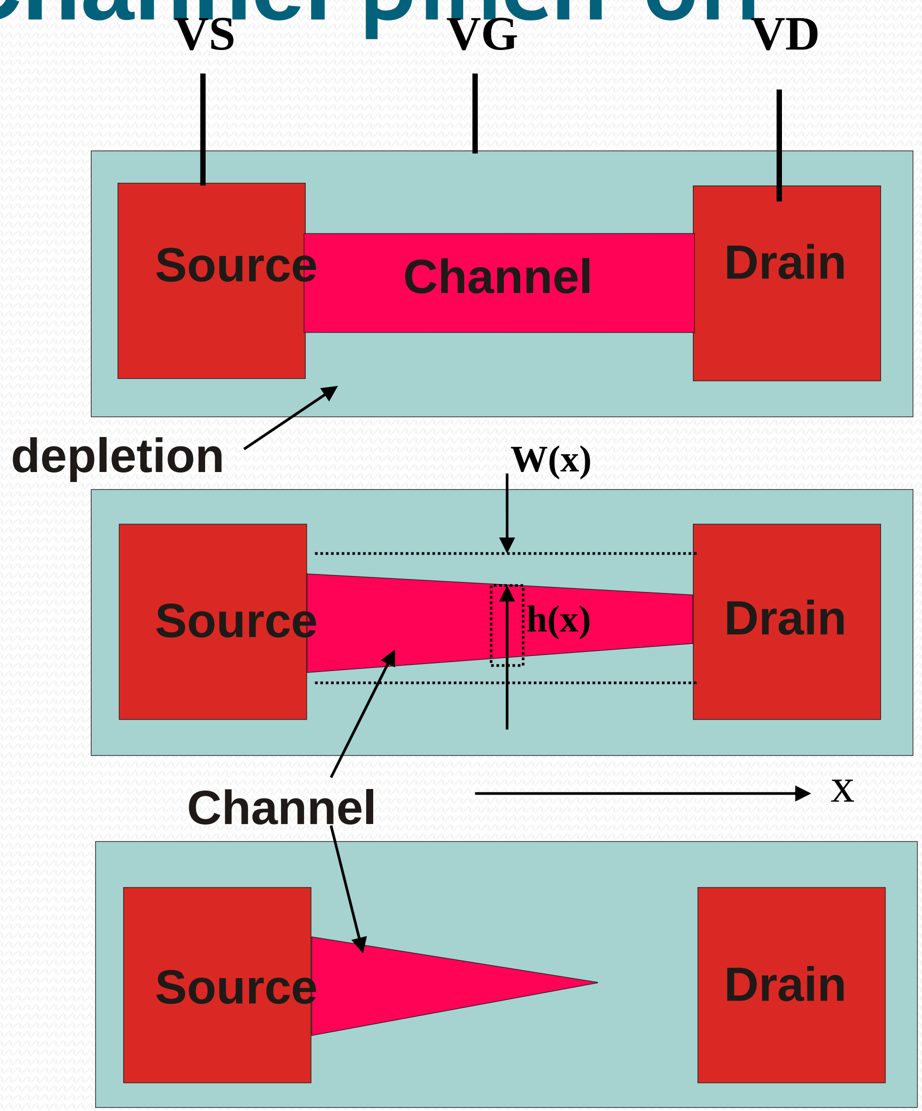
- an inversion layer (induced by band bending at junction, or charge accumulation with electrostatic force)

- surrounded by non-conducting region, usually by depletion region with an opposite carrier.

Example of a channel simulation



Channel pinch-off



Local resistor: $R = \frac{\rho}{Dh(x)} \Delta x$

Local voltage drop:

$$\Delta V_x = I_D R = I_D \frac{\rho}{Dh(x)} \Delta x$$

Local channel aperture:

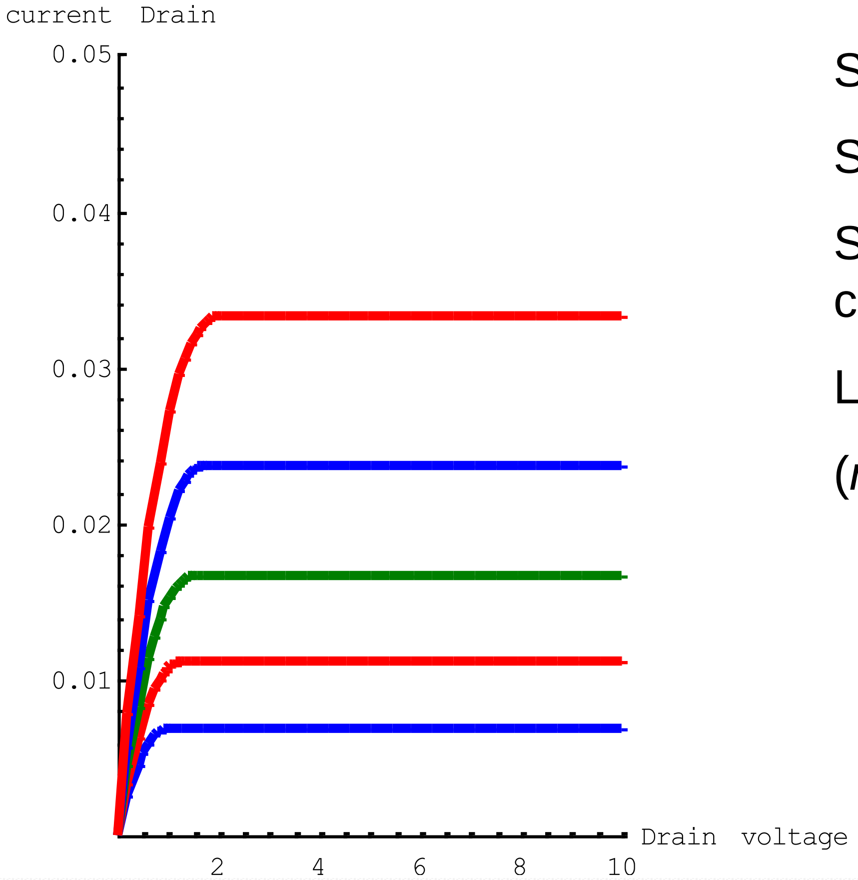
$$h(x) = h_o - 2W(x)$$

Pinch-off is a function of local voltage:

$$W(x) = f[V(x)] \cong h_o \sqrt{\frac{V(x) - V_G}{V_P}}$$

(we define: G0=D h0/(L r)): channel conductance

Approximation of I_D saturation:



Some simplistic approximations

Saturation is an approximation

Simplistic channel length and constant conductivity

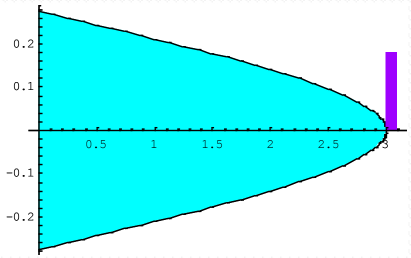
Low field and low current approximation

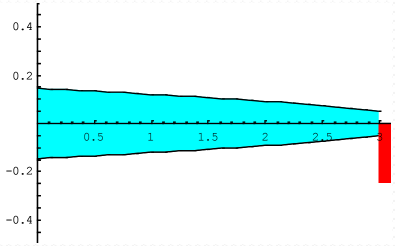
(*note the nonlinear saturation ID vs. gate*)

Key features: pinch-off and saturation is caused by the combination of drain voltage and gate on the channel

Generic FET summary

- The current between source and drain is controlled by a gated channel
- The channel conductive aperture can be spatially pinched-off by an electric field
- The pinch-off is a function of both the potentials between drain and source and the drain/source and gate, resulting in a saturable drain-source current
- The saturation current can be controlled by the gate potential



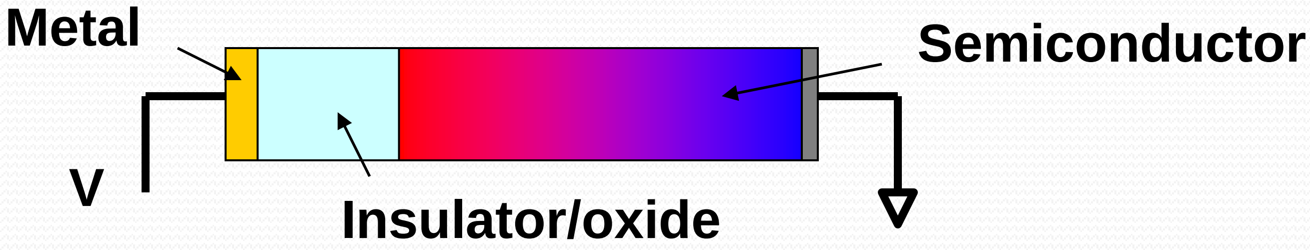


The engineering of the channel is practically the engineering of the FET: ***most R&D on FET are concerned with the design, fabrication, and physics of the channel***

It's all in the channel!

The physics of the mosfet channel

Metal oxide semiconductor junction



- It is a capacitor: charge accumulation at interface
- Interface charge is the carrier of the channel!

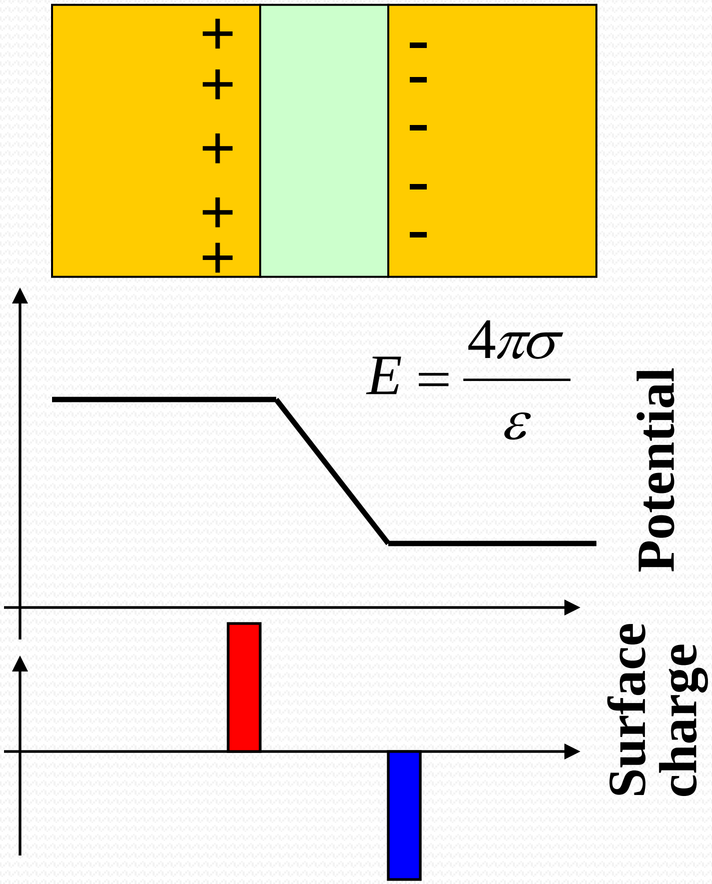
- To understand the charge: need to understand junction

- Junction of dissimilar materials: heterojunctions:

  - semiconductor/semicond. (different)
  - metal/semicond., insulator/semicond.
  - metal/oxide/semiconductor

Comparison of junctions

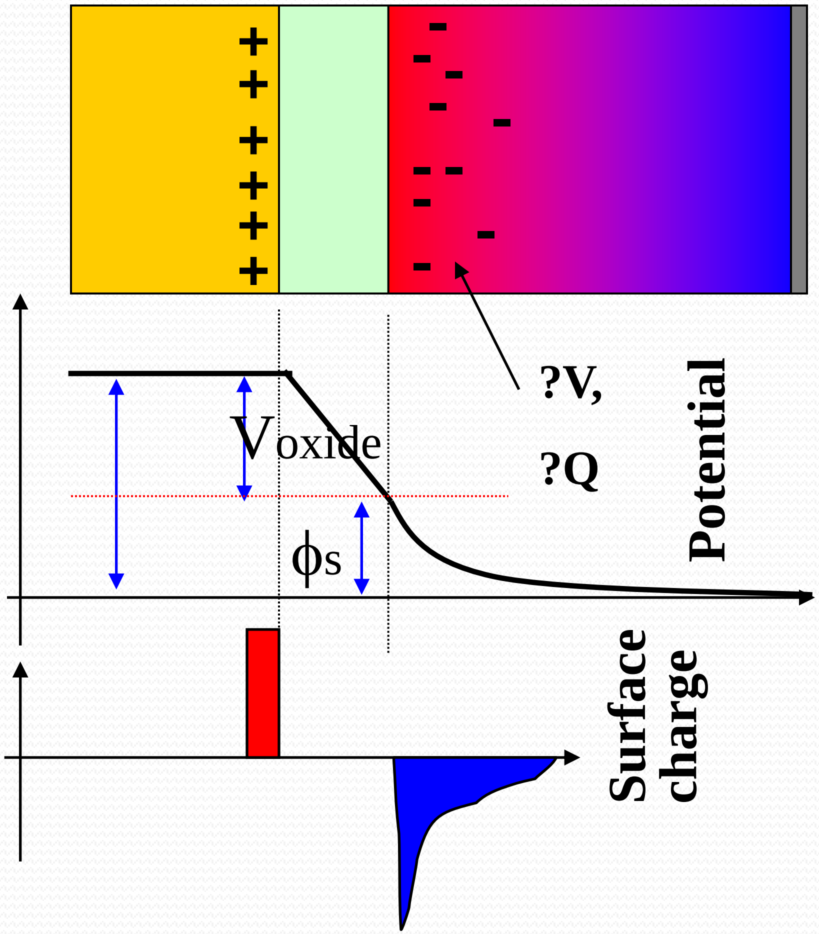
Metal-insulator-metal



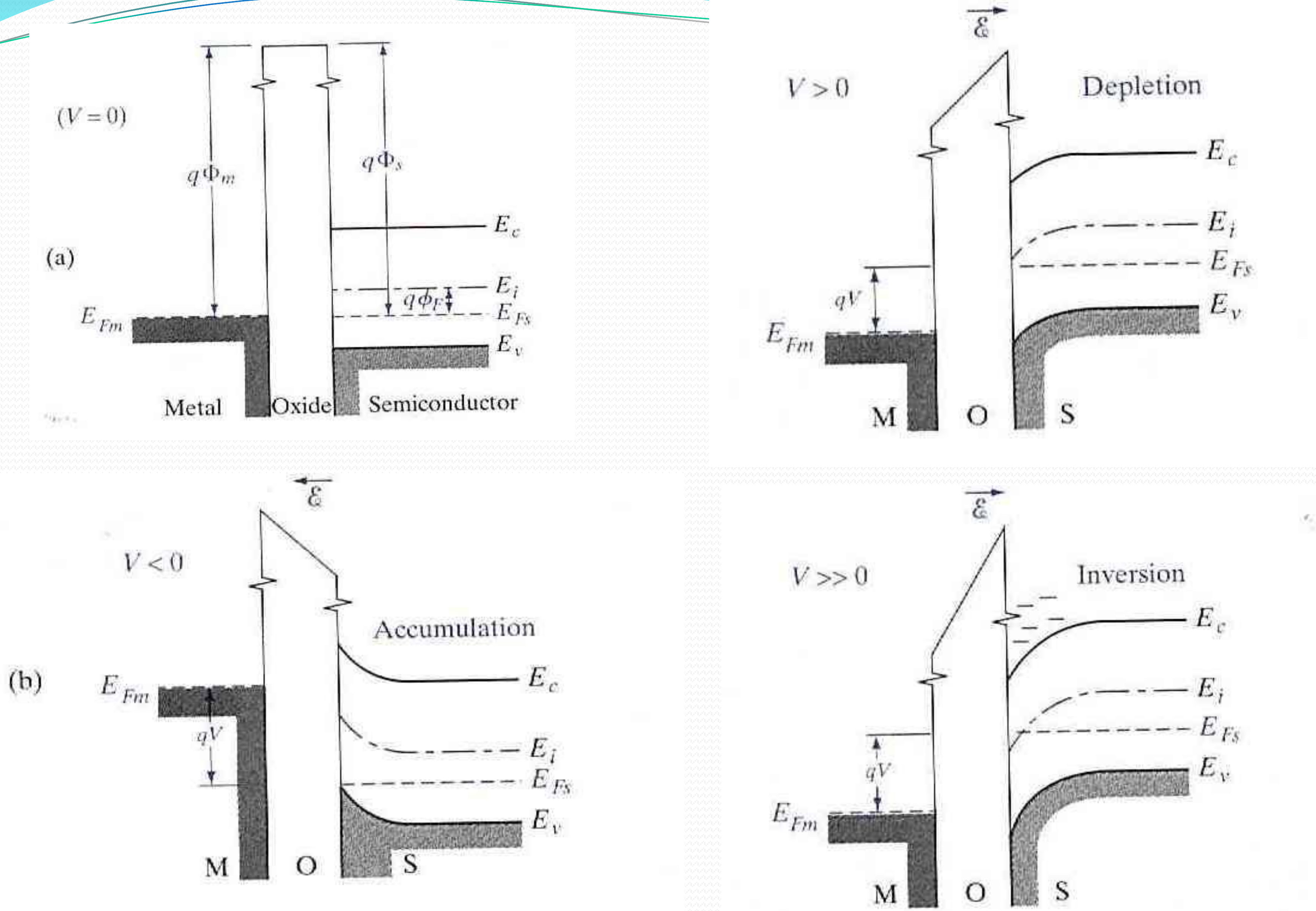
$$V = Ed = \frac{4\pi\sigma}{\varepsilon}d = \frac{4\pi Q}{\varepsilon A}d$$

$$C = \frac{Q}{V} = \frac{\varepsilon A}{4\pi d}$$

Metal-insulator-semiconductor



What does the junction behave like?



(V = 0)
(a)
qΦm
qΦs
qφF
EFm
Ec
Ei
EFs
Ev
Metal
Oxide
Semiconductor
V > 0
Depletion
qV
Ec
Ei
EFs
Ev
EFm
M
O
S
(b)
V < 0
Accumulation
EFm
qV
Ec
Ei
EFs
Ev
M
O
S
V >> 0
Inversion
Ec
Ei
EFs
Ev
qV
EFm
M
O
S

Key features of MOS channel

- It is a highly voltage-dependent capacitor
- With a bias opposite to the carrier type, a region devoid of majority carrier is developed in the semiconductor, called depletion region, which grows wider with higher bias
- At sufficiently strong bias, above a quantity called threshold bias, there is an accumulation of mobile charge of minority type: these are FET channel carriers
- This mobile charge layer is called inversion layer
- Increasing bias will result mostly more accumulation of inversion layer carriers, the depletion region hardly extends any further

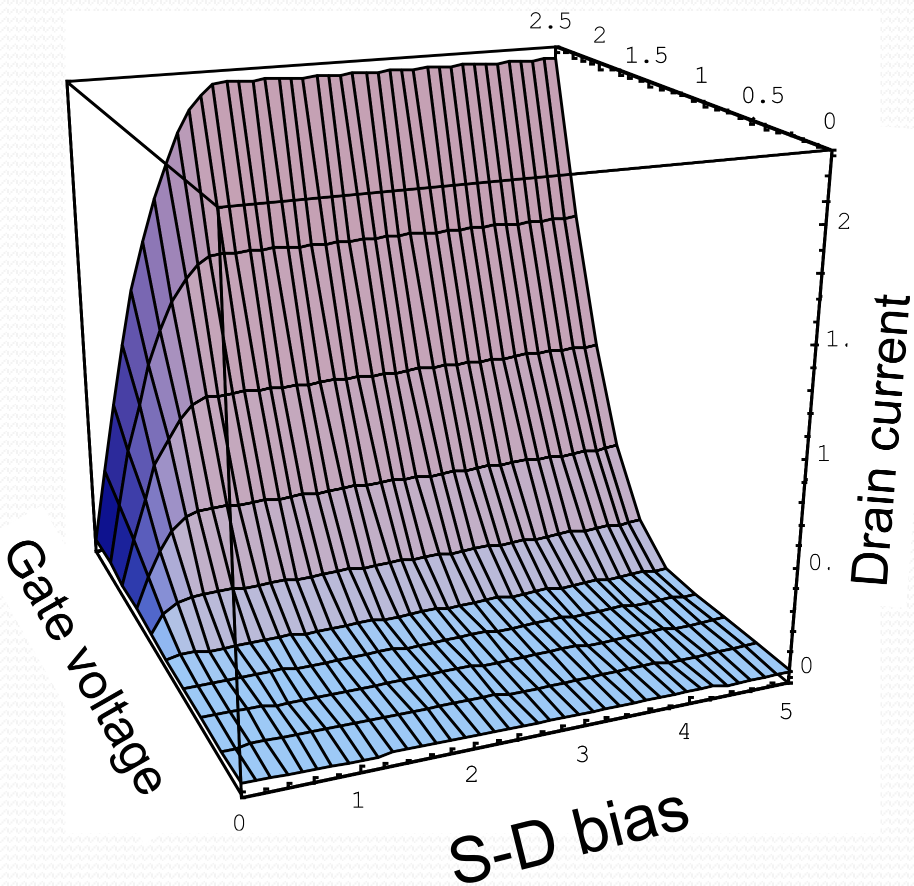
FET and BJT

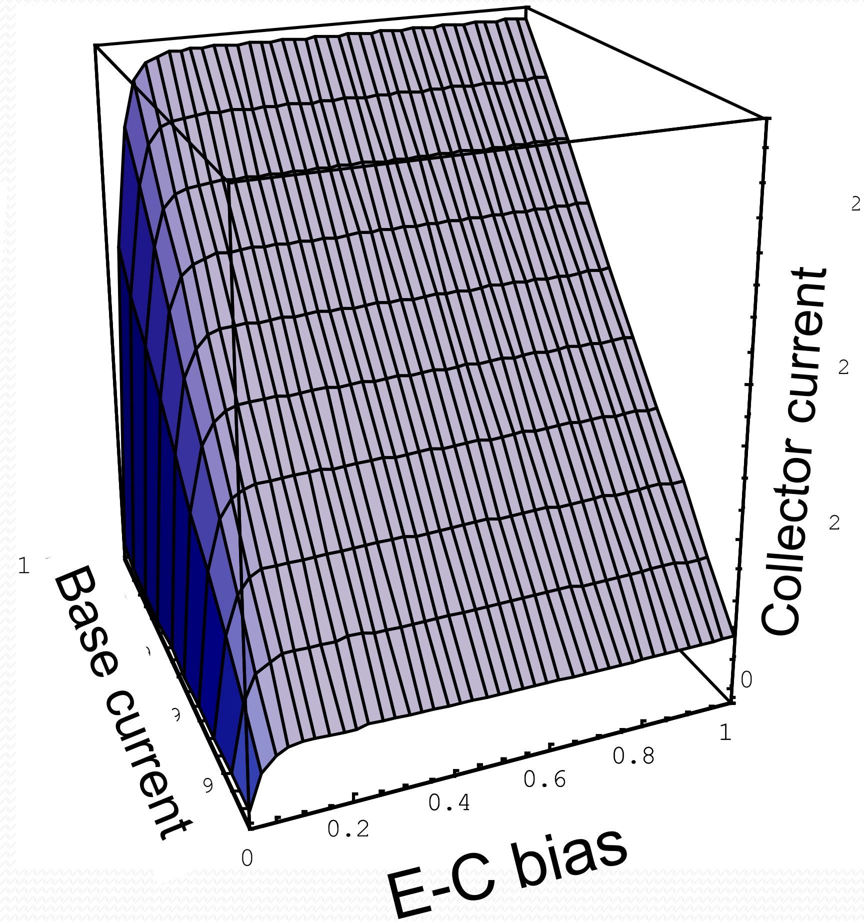
An comparative overview

FET vs. BJT: main features

FET	BJT
Source (S), gate (G), drain (D)	Emitter (E), base (B), collector (C)
IT'S ALL IN THE GATE CHANNEL!	IT'S ALL IN THE BASE!
Channel (underneath the gate) provides carriers for S-D	Base does NOT contribute (much) carriers nor current to the E-C current
Channel serves as a transport medium (D current comes from current provided from S)	Base serves as a transport medium (C current comes from E carriers)
But G does NOT provide (much) current to S-D current	**<u>There is a B current, usually small but crucial</u>** to the control of currents between E and C
<u>There is a "critical" G voltage</u> (threshold bias VT) for the transistor to be ON	There is no need for any "threshold" B voltage or current for the transistor to be ON
A "relatively" abrupt change from non-conductive to conductive state at VT	B current controls E-C current like a "lever" (small force lifts big force) – gradual
Above threshold, channel charge accumulation is linear vs. gate voltage	E current is exponential vs. B voltage. Linear control is by B current
Device design and engineering: gate oxide (or insulator) and channel	Device design and engineering: B length, carrier diffusion, E doping, length, carrier diffusion

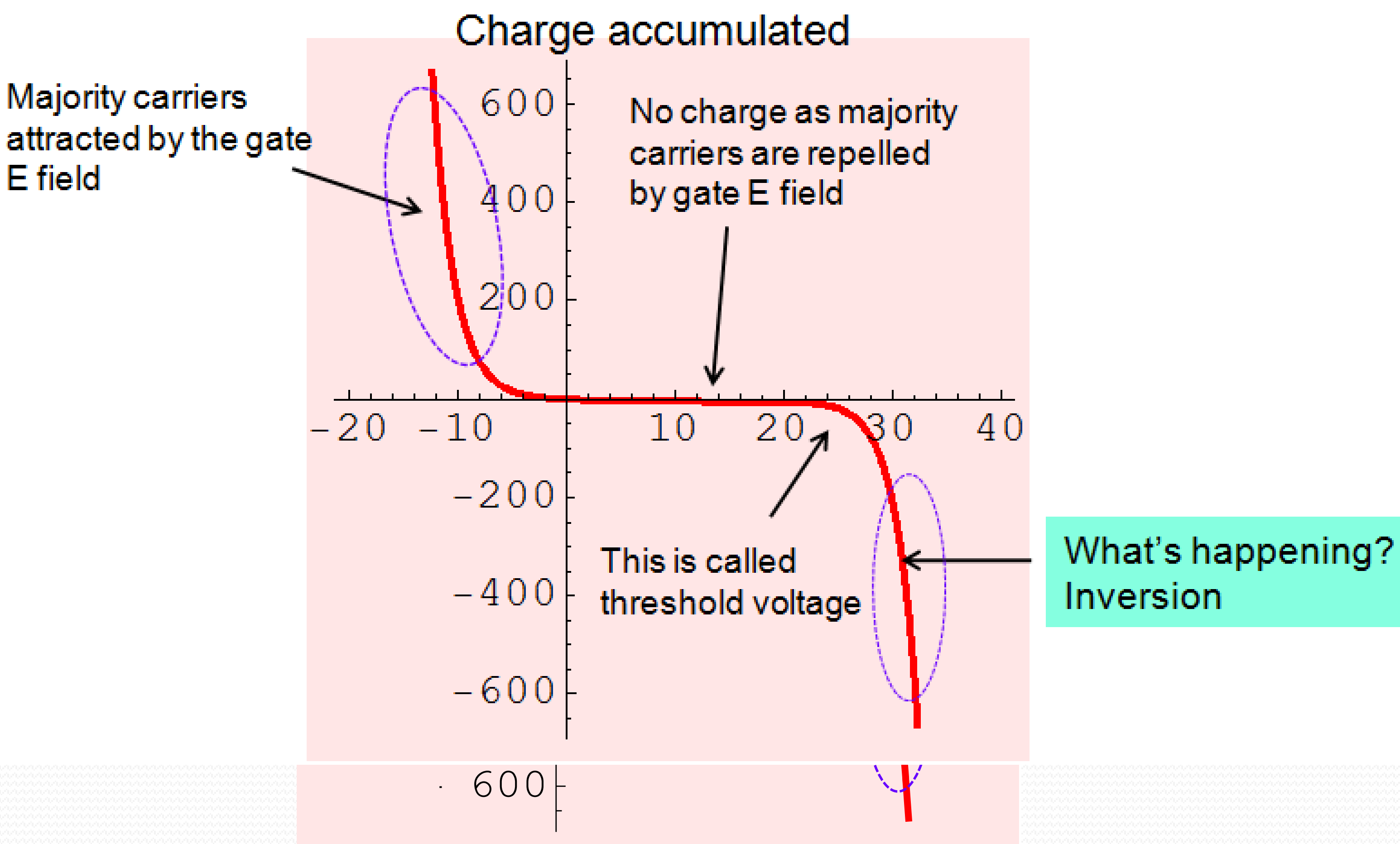
I-V characteristics of FET vs. BJT



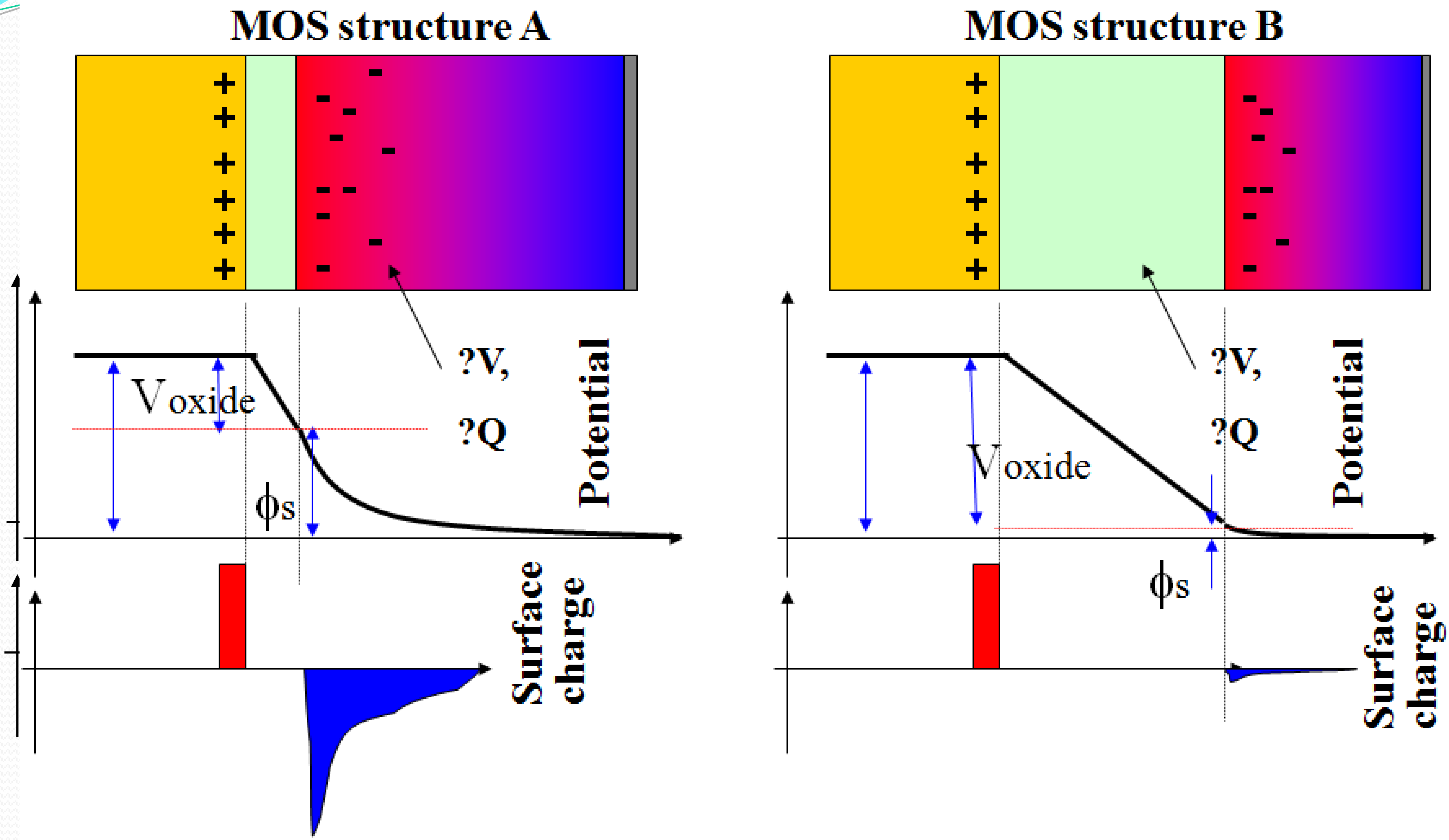


We must know and understand:

- The basic device physical structures (S-G-D for FET and E-B-C for BJT)
- The basic steps in fabrication these transistors:
  - elements of lithography: photoresist, mask, projection, baking, developing…
  - altering the semiconductors by doping (ion implantation, diffusion…)
  - oxidation, deposition of insulator layer for FET channel
  - metalization (metal deposition), Ohmic contact
- The basic concepts of the device operation of these transistors
  - for FET: how gate voltage can control the current between the source and drain (Gate bias voltage threshold, channel conductivity above and below threshold, pinch-off, source-drain current and current saturation)
  - for BJT: how base current can control the emitter majority carrier current, and the transport (base transport factor) to collector
- The physical principles in the operation of these transistors:
  - for FET: carrier behavior in the channel as a function of gate voltage: weak-field screening, depletion, inversion; mobile charge, non-mobile charge; related C-V characteristics, role of oxide (or insulator) capacitance;
  - for BJT: effects of base current (both majority and minority carriers).
  - for both: carrier mobility, temperature effects, doping effects
- Fundamental engineering principles of these transistors:
  - for FET: doping type, level, profile, oxide or insulator capacitance (dielectric constant, thickness) and efficiency in gate voltage
  - for BJT: doping type, level, profile; base length, carrier mobilities in base, diffusion lengths; minority carrier behaviors in emitter, emitter length, and emitter efficiency


Charge accumulated
Majority carriers attracted by the gate E field
No charge as majority carriers are repelled by gate E field
This is called threshold voltage
What's happening? Inversion
600
400
200
-200
-400
-600
-20
-10
10
20
30
40
600

Comparison of MOS structures



Which one will reach inversion with least gate voltage?