

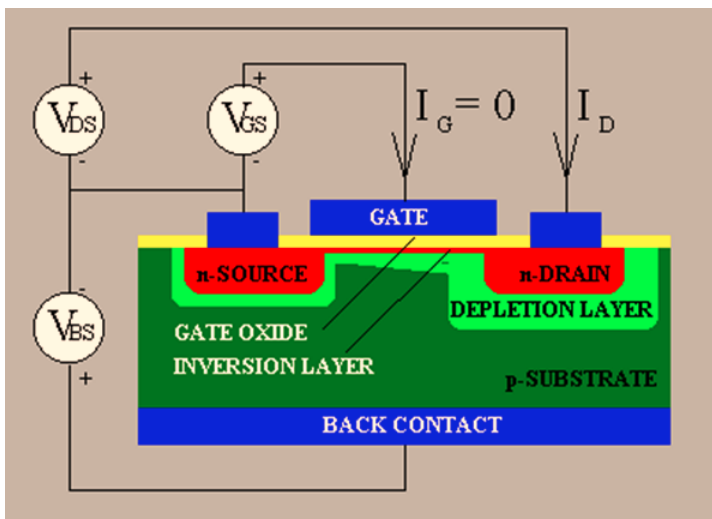
# Homework 6

ECE 4339

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## 1. (70 pts) MOSFET review

You are expected to generate graphs (use Apps) and explain the following questions. You don't have to do any computation unless you want to. But **the key idea is graphical explanation**. Feel free to use hand sketch pointing arrows, annotation, etc. on graphs to explain your points or ideas. Of course you can copy and edit your graphs in any graphic software such as ppt to add your annotation.



### 1.1 (10 pts) Depletion region in MOSFET

In the above MOSFET diagram, we see depletion all around. We understand the depletion region between the n-doped SOURCE and DRAIN vs. the rest p-doped substrate. But use App 1, you will notice a depletion region is also developed between channel electrons and holes. Not only that, the depletion region is NOT at a fixed location like a junction, but it moves as GATE voltage is applied. Illustrate using the App and explain why so?

**Hint:** it obeys the same rule about  $n_0 p_0$  product, except now we have  $n[x; V_G] p[x; V_G]$  which is a function of location within the channel and GATE voltage  $V_G$ . Using Log plot of carrier density, you can see what happens in the depletion region.

### 1.2 (10 pts) How important is the insulator layer thickness

Use appropriate Apps (you choose and decide) to explain the role of insulator layer thickness in MOSFET performance.

### 1.3 (10 pts) How important is the insulator dielectric $k$

Why do people want high  $k$ ? Use appropriate Apps (you choose and decide) to explain the role of insulator dielectric constant in MOSFET performance.

### 1.4 (20 pts) Fermi level

How does Fermi level affect MOSFET performance? Note that in the Apps, we define the parameter for Fermi level as  $E_i - E_f$ , not the Fermi energy  $E_f$  itself; and  $E_i$  is the intrinsic Fermi level. Hence,  $E_i - E_f > 0$  means that  $E_f$  is close to the valence band, and the larger it is, the more p-type it becomes. What how the threshold potential inside the semiconductor varies as a function of Fermi level  $E_i - E_f$ .

If low  $E_i - E_f$  means low GATE threshold (which is obviously an advantage), why don't we make it as low as intrinsic? Can you think of some disadvantage if we do so?

### 1.5 (20 pts) Active channel

We touch just a little about active channel. An App allows you to turn on DRAIN voltage to see what happens. The model is only for long channel FET ( $\sim 1 \mu\text{m}$  and longer), but it is useful to understand the pinch-off effect at DRAIN end of the channel. Explain your best understanding of what happens when we have pinch-off and DS current is saturated.

Note: DS current can never be saturated if we also include minority carrier current in CHANNEL (very small) that always exists even if GATE is off. So, pinch-off only means inversion carrier density drops below the channel minority carrier density  $\frac{n_i^2}{p_0}$  (which is very small, of course). Note the disadvantage of DS current leakage if we have low  $p_0$ .

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## 2. (30 pts+ 10 pts bonus) MOSFET practical

Here, you will apply what you learn to a practical problem: understand the specification sheet of a MOSFET. Supposed you are an engineer designing some circuit. You consider some MOSFET for power application (not for logic). But to use the device intelligently, it is essential to understand its behavior. Use what you learn from the MOSFET chapter to explain this spec sheet.

Download the spec sheet "*FDW2501N Fairchild N-channel MOSFET*" from the download page.

### 2.1 (2 pts)

Identify all the pins (1,2,3,4) with the contacts of the MOSFET (e. g. GATE, DRAIN, ...)

### 2.2 (2 pts)

What is the maximum drain-source current and dissipated power according to the datasheet?

### 2.3 (2 pts)

From 2.2 above, what is the effective internal load (or resistance) of the device? Compare this to the DRAIN-SOURCE (DS) resistance. Any comments?

## 2.4 (4 pts)

When GATE is off, and you apply 16 V across DRAIN and SOURCE, what is the current? What is the effective “resistance” under this condition? What is the ratio of this “gate-off” DS resistance to gate-on DS resistance? (Note discussion in question 1.5 above)

## 2.5 (10 pts)

Refer to Fig. 2: First, explain qualitatively (a paragraph) how the DS resistance increases fast vs. DS current for  $V_{GS} = 2$  V, but is nearly constant for  $V_{GS} > 3$  V? Then, next, use a **simple quantitative model** (from lecture or Apps) **and plot** to show such a behavior (only similar, not exactly).

## 2.6 (10 pts+10 pts bonus)

Refer to Fig. 7: Gate charge characteristics: Consider the operation point at  $V_{GS}=3$ V,  $V_{DS}=10$  V. If we assume the channel mobility  $\sim 200$  cm<sup>2</sup> / V s, what do you think the channel length approximately is?