Integrated Circuits
Integrated Circuits

- Its importance is well-known
- Invention of Jack Kilby and Robert Noyce

A scientific milestone: first transistor (Bell Labs 1947)

A technological milestone: Kilby’s integrated circuit, TI (1959)
Milestones

- 1959: First IC
- ... then a lot of nice ICs,...but they “can’t change much” (not programmable)

ENIAC
Op Amp

Source: wiki
Honeywell kitchen computer

<table>
<thead>
<tr>
<th>TECHNICAL INFORMATION</th>
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<tbody>
<tr>
<td>NAME</td>
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<tr>
<td>MANUFACTURER</td>
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<tr>
<td>TYPE</td>
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<td>ORIGIN</td>
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<tr>
<td>YEAR</td>
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<tr>
<td>BUILT IN LANGUAGE</td>
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<tr>
<td>KEYBOARD</td>
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<tr>
<td>CPU</td>
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<tr>
<td>SPEED</td>
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<td>RAM</td>
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<td>ROM</td>
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<td>TEXT MODES</td>
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<tr>
<td>SIZE / WEIGHT</td>
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<td>BUILT IN MEDIA</td>
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<td>POWER SUPPLY</td>
</tr>
<tr>
<td>PERIPHERALS</td>
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<tr>
<td>PRICE</td>
</tr>
</tbody>
</table>
Milestones

- 1971: Microprocessor: The story of Intel & Busicom, Ted (Marcian) Hoff
  - Silicon-gated MOS
  - 4004 with ~2000 transistors

What drive technology?
Technology Cycles - Wealth Creation / Destruction
New Companies Often Win Big in New Cycles

**Mainframe Computing 1950s**
- IBM
- NCR
- Control Data
- Sperry
- Honeywell
- Burroughs

**Mini Computing 1960s**
- Digital Equipment
- Data General
- HP
- Honeywell
- Prime
- Computervision
- Wang Labs

**Personal Computing 1980s**
- Microsoft
- Cisco
- Intel
- Apple
- IBM
- Oracle
- EMC
- Dell
- HP
- Compaq

**Desktop Internet Computing 1990s**
- Google
- AOL
- eBay
- Yahoo!
- Yahoo! Japan
- Amazon.com
- Tencent
- Alibaba
- Baidu
- Rakuten

**Mobile Internet Computing 2000s**

Note: Winners from 1950s to 1980s based on Fortune 500 rankings (revenue-based), desktop Internet winners based on wealth created from 1995 to respective peak market capitalizations. Source: Factset, Fortune, Morgan Stanley Research.

Source: Mary Meeker
“Smart” ICs

Field Programmable Gate Array (FPGA)

Digital Signal Processor (DSP)

Microprocessor
FPGA vs. Microprocessor

- IC technology supports very diverse architecture
The “Old-Time Story” of RISC vs. CISC

- Specialized architectures for different applications

ARM

x86
Memory IC’s

SRAM

DRAM

Non-volatile RAM

NAND flash SSD
<table>
<thead>
<tr>
<th>Microprocessor</th>
<th>Year of Introduction</th>
<th>Transistors</th>
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<tbody>
<tr>
<td>4004</td>
<td>1971</td>
<td>2,300</td>
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<tr>
<td>8008</td>
<td>1972</td>
<td>2,500</td>
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<tr>
<td>8080</td>
<td>1974</td>
<td>4,500</td>
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<td>8086</td>
<td>1978</td>
<td>29,000</td>
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<tr>
<td>Intel 286</td>
<td>1982</td>
<td>134,000</td>
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<td>Intel 386™ processor</td>
<td>1985</td>
<td>275,000</td>
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<td>1989</td>
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<td>1999</td>
<td>9,500,000</td>
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<td>Intel® Pentium® 4 processor</td>
<td>2000</td>
<td>42,000,000</td>
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<td>Intel® Itanium® processor</td>
<td>2001</td>
<td>25,000,000</td>
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<tr>
<td>Intel® Itanium® 2 processor</td>
<td>2003</td>
<td>220,000,000</td>
</tr>
<tr>
<td>Intel® Itanium® 2 processor (9MB cache)</td>
<td>2004</td>
<td>592,000,000</td>
</tr>
</tbody>
</table>
Moore’s law

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

curve shows transistor count doubling every two years


Date of introduction

Transistor count

Source: Wiki
Microprocessor Cost Per Transistor Cycle

Logarithmic Plot

Halving time: 1.1 years
Key Enabling Technologies For ICs
Crucial elements of IC technology

- Devices and materials
  - Transistor design and scaling
  - Semiconductors and advanced materials
- Fabrication technology (Front end):
  - feature size: how small can a transistor gate be?
  - how to pack many T’s in a very small area: VLSI, ULSI
  - device structure: beyond planar, 2D constraint
  - how to make high-performance oxides, insulators
  - how to make contact, “wiring”?  
  - wafer scaling
- Chip packaging technology (Back end)
Focus of this talk: emerging nanoelectronic devices

Source: Robert Chau, Intel

Note: Future options subject to change
Moore’s Law Requires More Than Just Scaling

- **2003**: 90nm
- **2005**: 65nm
- **2007**: 45nm
- **2009**: 32nm
- **2011**: 22nm

- **130nm (2001)**
  - Scaling

- **Materials Science**
  - Strained Silicon >3yrs
  - High-k Metal Gate >3.5yrs
  - Tri-Gate 4yrs?

- **1st Competitor**

- **www.semiaccurate.com**
How small can the transistor be?

*Past prediction*

The ultimate limit of the transistor is \(~ 10 \, \mu m\)

1961

... On a pentium (~2002), it was \(~ 0.1 \, \mu m\)

... And they think: 0.015 \, \mu m is the ultimate limit

*Don’t bet your money on it!*
Transistor Physical Gate Length Trend (Lithography generation > L_{GATE})

Year


Micron

0.5µm 0.35µm 0.25µm 0.18µm 0.13µm

0.2µm 130nm 0.13µm 90nm

0.2µm 0.18µm 0.13µm 90nm

Technology Node

Transistor Physical Gate Length

15nm 20nm 30nm 45nm 65nm 90nm
Transistor Scaling Continues

In 2005

70nm transistor (in production)

30nm transistor (production 2005)

20nm transistor (research phase)
Introducing 14XM (eXtreme Mobility)

Foundry’s first innovative 14nm FinFET
Our solution is focused on:
- Rapid Time to Market (TTM)
- Ultra-Low Power
- Lowest risk path to high-volume manufacturing
- Competitive Cost and Performance

In production

bsn*

In development
In 2010

Newest Manufacturing Technology Delivers Ivy Bridge

- 45 nm Process Technology
  - Penryn
    - Intel® Core™ Microarchitecture
  - Nehalem
    - NEW Intel® Microarchitecture
- 32 nm Process Technology
  - Westmere
    - Intel® Microarchitecture (Nehalem)
  - Sandy Bridge
    - NEW Intel® Microarchitecture
- 22 nm Process Technology
  - Ivy Bridge
    - Intel® Microarchitecture (Sandy Bridge)
    - Intel’s First 22 nm Processor

Cadence of Innovation Delivers New Microprocessor Efficiency on the 22 nm Process

intel
Intel R&D Pipeline

2011

22 nm

IN PRODUCTION

2013

14 nm

IN DEVELOPMENT

2015+

10 nm 7 nm 5 nm

IN RESEARCH

Lithography • Materials • Interconnect
... and more

Innovating for the Next Decade of Computing

Source: Intel

Investing for the Future
Dynamic RAM
Smallest (called “Half Pitch”) Feature Size

Logarithmic Plot

$\frac{y}{y_0} = 0.9901$

Halving time: 5.4 years

Dual logics: CMOS
CMOS: a key to VLSI/ULSI

Remember HW on p-channel?

Source: wiki
Why CMOS?

- Threshold voltage requirement: voltage drop in each stage: example: n-channel

\[ V_{DD} \rightarrow V_{DD} - V_t \]

- n-channel MOSFET is “natural” for logic 0 (ex. ON: +5 V), p-channel MOSFET is “natural” for logic 1 (ex. OFF: +5 V). Together: CMOS
CMOS example: NAND

Source: wiki
Shrinking devices require increasing resolution lithography
Conventional Lithography (simplified)

Light source

Mask

4:1 reduction lens

Pattern produced on wafer

Conventional lithography has its limits

- Resolution adequate for 0.10 μm process, but no further
- Like trying to fill out a checkbook with a crayon

intel
Figure 2 The lens for DUV photolithography with the highest NA: Starlith 1900 from Carl Zeiss. The height of the lens is more than 1 m. The optical design and ray path are schematics and given only as an illustration. The inset depicts a resist structure of 36.5-nm half-pitch, obtained with the lens at full scanning speed. Main image courtesy of Zeiss; inset courtesy of ASML.
Lithography Challenge

Minimum feature size is scaling faster than lithography wavelength
Advanced photo mask techniques help to bridge the gap
What is Extreme Ultraviolet Lithography (EUVL)?

- EUV lithography uses extremely short wavelength light (factor of 20 shorter than today’s lithography processes)

  - Visible light – 400 to 700 nm
  - DUV lithography – 193 and 248 nm
  - EUV lithography – 13 nm

- Will be used first in 2005 by leading edge companies for critical lithography steps to produce 70 nm patterns for advanced circuit manufacturing to maintain Moore’s Law
ITRS lithography roadmap

Lithography friendly design rules

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<td>Innovative EUV, Imprint, ML2</td>
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</tbody>
</table>

Legend:
- **Black**: Research Required
- **Blue**: Development Underway
- **White**: Qualification/Pre-Production
- **Continuous Improvement**: Continuous Improvement

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.
Connecting devices at high density requires good conductor.
Metal Interconnect

- For many years... It has been aluminum
- 30+ years of research for a better conductor: copper
- Copper technology has finally arrived within the last 20 years...

Copper Interconnects

Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors

6 Layers of Damascene Copper
Price pressure: more devices per wafer – the advantage of economy of scale
More chips per wafer
The economy of scales

Large wafer...

Lots of chips (require high yield)
Chip architecture
Application/Market-driven

Not just size and integration, architecture is very apps-driven
The “Old-Time Story” of RISC vs. CISC

- Specialized architectures for different applications

ARM

x86
Intel vs. ARM

Intel Market Cap ~ $140 Billion

ARM Market Cap > $700 Billion

S. K. Jayanarayanan
kartik.jayan@gmail.com
March 2012
The fast evolving market
Technology is driven by the market & industrial players
### Top 10 IC Wafer Capacity Leaders* as of Dec-2013 (200mm-Equiv. Wafers per Month x1000)

<table>
<thead>
<tr>
<th>2013 Rank</th>
<th>Company</th>
<th>Headquarters Region</th>
<th>Installed Capacity (K w/m)</th>
<th>% of Worldwide Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Samsung</td>
<td>South Korea</td>
<td>1,867</td>
<td>12.6%</td>
</tr>
<tr>
<td>2</td>
<td>TSMC</td>
<td>Taiwan</td>
<td>1,475</td>
<td>10.0%</td>
</tr>
<tr>
<td>3</td>
<td>Micron**</td>
<td>Americas</td>
<td>1,380</td>
<td>9.3%</td>
</tr>
<tr>
<td>4</td>
<td>Toshiba/SanDisk</td>
<td>Japan</td>
<td>1,177</td>
<td>8.0%</td>
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<tr>
<td>5</td>
<td>SK Hynix</td>
<td>South Korea</td>
<td>1,035</td>
<td>7.0%</td>
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<tr>
<td>6</td>
<td>Intel</td>
<td>Americas</td>
<td>961</td>
<td>6.5%</td>
</tr>
<tr>
<td>7</td>
<td>ST</td>
<td>Europe</td>
<td>551</td>
<td>3.7%</td>
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<tr>
<td>8</td>
<td>UMC</td>
<td>Taiwan</td>
<td>520</td>
<td>3.5%</td>
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<tr>
<td>9</td>
<td>GlobalFoundries</td>
<td>Americas</td>
<td>482</td>
<td>3.3%</td>
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<td>10</td>
<td>TI</td>
<td>Americas</td>
<td>441</td>
<td>3.0%</td>
</tr>
<tr>
<td>—</td>
<td>Total</td>
<td>—</td>
<td>9,889</td>
<td>66.8%</td>
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</table>

*Includes shares of capacity from joint ventures.

Source: Companies, IC Insights

**Includes the former Elpida and Rexchip fabs.
Foundry and Chip Design

http://www.techbriefs.com/component/content/article/15547
Foundry Capacity by Technologies

- 28nm
- 40nm
- 65nm
- 90nm
- 0.13um
- 0.18um
- 0.25um
- 0.35um
- 0.5um

Gartner
### Worldwide Capacity by Minimum Geometry as of Dec-2012

(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)

<table>
<thead>
<tr>
<th>Minimum Geometry</th>
<th>Installed Capacity (K w/m)</th>
<th>% of Worldwide Total</th>
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</thead>
<tbody>
<tr>
<td>&lt;40nm</td>
<td>3,963.1</td>
<td>27.3%</td>
</tr>
<tr>
<td>&lt;60nm – ≥40nm</td>
<td>2,721.0</td>
<td>18.8%</td>
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<tr>
<td>&lt;80nm – ≥60nm</td>
<td>1,106.6</td>
<td>7.6%</td>
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<tr>
<td>&lt;0.2μ – ≥80nm</td>
<td>3,165.5</td>
<td>21.8%</td>
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<tr>
<td>&lt;0.4μ – ≥0.2μ</td>
<td>1,495.8</td>
<td>10.3%</td>
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<tr>
<td>≥0.4μ</td>
<td>2,044.9</td>
<td>14.1%</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>14,497.0</strong></td>
<td><strong>100%</strong></td>
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Source: IC Insights
## Worldwide Capacity by Geographic Region as of Jul-2011
(Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)

<table>
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<th>Region</th>
<th>Installed Capacity (K w/m)</th>
<th>% of Worldwide Total</th>
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<td>Americas</td>
<td>1,995.1</td>
<td>14.7%</td>
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<tr>
<td>Europe</td>
<td>1,109.3</td>
<td>8.1%</td>
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<tr>
<td>Japan</td>
<td>2,683.6</td>
<td>19.7%</td>
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<tr>
<td>Korea</td>
<td>2,293.5</td>
<td>16.8%</td>
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<tr>
<td>Taiwan</td>
<td>2,858.3</td>
<td>21.0%</td>
</tr>
<tr>
<td>China</td>
<td>1,208.9</td>
<td>8.9%</td>
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<tr>
<td>ROW</td>
<td>1,469.2</td>
<td>10.8%</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>13,617.8</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

Source: IC Insights
Perspectives from industrial players
Brief Update on 14nm Status

Yield at the same point in development

Yield rapidly increasing, on track for matched yield in Q1 '14 *

Performance Improvement
Switching Energy vs. Gate Delay

Switching Energy Change (%)

Delay Change (%)
Getting Benefits of Moore’s Law Across all Value Vectors

Lower Cost

Active Power per Function

Lower Power

Higher Performance

Source: Intel
Different Improvement Focus for Different Segments

**Performance**
- 2x Performance Improvement for Server
- 1x Performance Improvement for Laptop
- 1x Performance Improvement for Mobile

**Active Power**
- Active Power Reduced (Includes performance increase)
- 1x Active Power Improvement for Server
- .25x Active Power Improvement for Laptop
- .25x Active Power Improvement for Mobile

**Performance per Watt**
- Performance per Watt Improves >1.6x per Generation
Three Key Technology Enablers

- **Lithography Enabled**
  - Density
  - Power / Performance
  - Cost

- **Materials Enabled**
  - Power / Performance
  - Strained Silicon
  - High K / Metal Gates
  - FinFETs

- **3D enabled**
  - Density
  - Functionality
  - Integration
Low Power Is Critical For Mobility Market

Explosive growth in smartphone sales

<table>
<thead>
<tr>
<th>Year</th>
<th>Shipments (in M units)</th>
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<tbody>
<tr>
<td>2009</td>
<td>178</td>
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<tr>
<td>2010</td>
<td>298</td>
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<tr>
<td>2011</td>
<td>471</td>
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<tr>
<td>2012</td>
<td>654</td>
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<tr>
<td>2013</td>
<td>841</td>
</tr>
</tbody>
</table>

Source: Gartner

New consumer appetite, driving more compute

Average daily use of smartphone

- 10 minutes (12%) Web/Web Apps
- 27 minutes (32%) Telephony
- 4 minutes (5%) Maps
- 4 minutes (5%) Games
- 7 minutes (9%) Messages
- 40 minutes (47%) All Other
- 7 minutes (9%) Social Networking
- 7 minutes (9%) Utilities
- 7 minutes (9%) More

Source: KPCB

60% time spent on smartphones is new activity for mobile users

...However, battery technology fails to keep up with Moore's law

Performance versus battery life improvement in smartphones

- Cortex A15
- Quad core
- 20,000 DMIPS

Source: GLOBALFOUNDRIES
Product Leadership Is More Than “Just The Fin”

- Full suite PDK
  - FinFET models, advanced extraction, double patterning, DFM, FFM, Ref flows, P&R…

- Mobile SoC platform
  - Optimized libraries, IPs suite, low power flow…

- 14XM
  - Power/Perf optimized CPU Solutions
    - Multi Vt, DVFS, power management, CPU POP…
  - Multicore GPU solutions
    - UHD 8T std cells, GPU POP…
  - CCS platform
    - (CCS=Compute, Connect, Storage)
    - Optimized libraries, IPs suite, HD memory solution, HS SERDES…
  - 2.5D and 3D Packaging
    - Logic+memory, wide IO, Heterogeneous Stacking…

Globally Foundries
* Source: Samsung Electronics Co., Ltd.

*Vdd*: Supplying voltage of drain
TSMC Technology Roadmap

TSMC technology leadership for SoC and mobile computing:
- Speed * Gate density
- Energy efficient transistors and interconnect

Production

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
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<tr>
<td>CLN65/55GP</td>
<td>CLN28HPM (HKMG)</td>
<td>CLN20SOC (Planar)</td>
<td>CLN16FF (FinFET)</td>
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Box left edge: risk production. Right edge: no meaning
10nm preliminary subject to change
The battle of chip architecture
Intel vs. ARM

Intel Market Cap ~ $140 Billion

ARM Market Cap > $700 Billion

S. K. Jayanarayanan
kartik.jayan@gmail.com
March 2012
ARM Business Model

ARM licenses technology to Partner

Partner develops chips

OEM sells consumer products

2-3 yrs to design new processor
3-4 yrs from license to royalty
Processor can ship for +20 yrs
Silvermont Highlights

Better Performance
- Out of Order Execution engine
- New multi-core and system fabric architecture
- New IA instructions extensions (Core™ Westmere level)
- New security and virtualization technologies

Better Power Efficiency
- Wider dynamic operating range
- Enhanced active and idle power management

Full Advantage of Intel® 22nm SoC Process Technology
- 3-D Tri-gate transistors tuned for SoC products
- Architecture and design co-optimized with the process

~3X the Performance or ~5X Lower Power†

†Based on the geometric mean of a variety of power and performance measurements across various benchmarks. Benchmarks included in this geometric are measurements on browsing benchmarks and workloads including SunSpider™ and page tests on Internet Explorer™, Firefox™, & Chrome™; Dhrystone™; GEOMB™ workloads including CoreMark™; Android™ workloads including Cinebench™, AirTube™, Unpack™ and Quadrant™ as well as measured estimates on SPECint® rate_base2006, SPECcpu® rate_base2006, on Silvermont preproduction systems compared to Atom processor 2308G. Individual results will vary. SPEC® CPU®2006® is a retired benchmark. * Other names and brands may be claimed as the property of others.
Exclusive: Intel Opens Fabs To ARM Chips

As the old adage goes, if you can’t beat them, join them. Well, that’s exactly what Intel finally decided to do relative to its lagging mobile business.

At the ARM developers conference today, Intel partner Altera announced that the world’s largest semiconductor company will fabricate its ARM 64-bit chips starting next year. The announcement sent shockwaves through the technology industry as Intel is desperately trying to break ARM’s supremacy in the mobile market. Unlike Intel, ARM Holdings of the U.K. doesn’t manufacture chips but its designs are licensed
Intel to make multi-die 14nm finfet devices with Altera

Altera and Intel are working together on the development of multi-die devices which integrate 14nm Stratix 10 FPGAs with memory, processors and analogue components in a single package.

The heterogeneous multi-die devices incorporate 3D silicon technology and Intel's 14nm Tri-Gate (finfet) process technology.

Intel is already manufacturing Altera's Stratix 10 FPGAs and system-on-chip devices (SoCs) using the 14nm Tri-Gate process.

Intel and Altera are currently developing test vehicles aimed at streamlining manufacturing and integration flows.

"Our partnership with Altera to manufacture next-generation FPGAs and SoCs using our 14nm Tri-Gate process is going exceptionally well," said Sunit Rikhi, vice president and general manager, Intel Custom Foundry.

"Our close collaboration enables us to work together in many areas related to semiconductor manufacturing and packaging," said Rikhi.

Together, both companies are building off one another's expertise with the primary focus on building industry-disrupting products.

According to Brad Howe, senior vice president of R&D at Altera, access to Intel's manufacturing and chip packaging capabilities is allowing the FPGA supplier to offer system-in-a-package products which are "critical to meeting overall performance requirements."

Related news:
Altera: 14nm Stratix and 20nm Arria FPGA details
Samsung teams with GlobalFoundries on 3D chips

Samsung is partnering with chip manufacturer GlobalFoundries to increase the supply of low-power, high-speed chips for smartphones and tablets.

GlobalFoundries has licensed Samsung’s 14-nanometer FINFET chip making process, which is used to manufacture 3D transistors. Those transistors will allow GlobalFoundries to make chips that are 20 percent faster and use 35 percent less power than chips made using its current 20-nanometer technology, the companies said.

GlobalFoundries doesn’t use the chips itself. It’s a foundry supplier, which means it makes chips for other companies that outsource their chip production, such as Advanced Micro Devices, Nvidia and Qualcomm.

Chip makers are constantly racing to build faster, more power-efficient chips, and the deal with Samsung will help GlobalFoundries compete better with other foundry suppliers such as Taiwan’s TSMC.

In fact, GlobalFoundries had been pursuing its own 14-nanometer technology, which it planned to introduce this year. It has now dropped that technology, apparently deciding that Samsung’s FINFET process is a better option.
The big customers
The growth cycle

1. More Computing-intensive demand
2. More powerful chips
3. Technology development
4. More affordable chips
5. More applications